Instruction Manual

Tektronix

TMS 810
Rambus Direct RIMM Memory Bus Support

071-0471-02

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Ground the Product. This product is indirectly grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

Use Proper AC Adapter. Use only the AC adapter specified for this product.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, switch off the instrument power, then disconnect the power cord from the mains power.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface

This instruction manual contains specific information about the TMS 810 Rambus Direct Support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating Microprocessor or bus support packages on the logic analyzer for which the TMS 810 Rambus Direct Support was purchased, you will only need this instruction manual to set up and run the support.

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that decodes bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a user manual covering the basic operations of Rambus Direct support.
- The term “logic analyzer” refers to the Tektronix logic analyzer for which this product was purchased.
- The term “HI module” refers to the module in the higher-numbered slot and the term “LO module” refers to the module in the lower-numbered slot.

  The portable logic analyzer has the lower numbered slots on the top and the benchtop logic analyzer has the lower numbered slots on the left.

Contacting Tektronix

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Service support	1-800-833-9200, select option 2*
Technical support	Email: techsupport@tektronix.com 1-800-833-9200, select option 3* 1-503-627-2400 6:00 a.m. – 5:00 p.m. Pacific time

* **This phone number is toll free in North America. After office hours, please leave a voice mail message.**
Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.

Getting Started

Getting Started

This chapter contains the following information on the TMS 810 Rambus Direct support package: configuring the probe adapter, connecting the logic analyzer to the system under test, and applying power to the probe adapter.

Support Package Description

The TMS 810 Rambus Direct support package displays disassembled data from systems based on the Rambus.

To use this support efficiently, refer to information on basic operations in your online help and the following documents:

- *Direct Rambus RIMM Module Specification, Rambus, Inc., 1998*
- *Direct Rambus Technical Description, Rambus, Inc., 1998*

Information on basic operations also contains a general description of support.

Logic Analyzer Software Compatibility

The label on the TMS 810 Rambus support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the TMS 810 Rambus support package you need a Tektronix logic analyzer equipped with the following modules: a combination of one 136-channel and one 102-channel, or two 136-channel modules. The 136-channel module must be in the lower numbered slot. The modules must be in adjacent slots and merged. The suggested module speed is a minimum of 100 MHz.

Requirements and Restrictions

Review electrical specifications in the *Specifications* chapter on pages 3–1 as they pertain to your system under test, as well as the following descriptions of other TMS 810 Rambus Direct support package requirements and restrictions.

System Clock Rate. The TMS 810 Rambus Direct support package can acquire data from the Rambus module operating at speeds of up to 400 MHz. The TMS 810 Rambus Direct support package has been tested to this clock rate. This specification is valid at the time this manual was printed. Contact your Tektronix sales representative for current information on the fastest devices supported.

Non-Intrusive Acquisition. The TMS 810 Rambus Direct probe adapter will not intercept, modify, or present signals back to the system under test.

Functionality Not Supported

Read Data. Read Data is not supported.

Range Recognizers. Range Recognizers are not supported.

Serial Presence Detect. Serial Presence Detect is not supported.

Control Register Transactions. Control register transactions, which use the SIO bus, are not supported, but Power State Transitions for NAP/PDN Exit, which also use the SIO bus, are supported. However, the TMS 810 Rambus Direct support package will only indicate power state transitions for NAP/PDN Exit, as indicated by the SIO bus, and will not track the present power state of the RDRAM devices.

Connecting the Logic Analyzer to the SUT

Your system under test (SUT); must have a minimum amount of clearance surrounding the Rambus Direct RIMM socket to accommodate the probe adapter.

To connect the logic analyzer to a system under test using the probe adapter, follow these steps:

1. Turn off power to your system under test. It is not necessary to turn off power to the logic analyzer.

CAUTION. *To prevent static damage, handle these components only in a static-free environment. Static discharge can damage the Rambus Direct probe adapter, the probes, and the logic analyzer module.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the Rambus Direct probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, before you remove the probe adapter from the protective bag it is shipped in, touch the bag to discharge stored static electricity from the probe adapter.
3. Place the system under test on a horizontal static-free surface.
4. Remove the Rambus Direct RIMM module from your system under test, using the latch release levers on the RIMM socket. Store the Rambus Direct RIMM module in a static free protective bag.
5. Remove the probe adapter from the protective packaging.

NOTE. *To prevent incorrect acquisition, both the probe adapter and the Rambus Direct RIMM connectors must be connected with their signal-flow moving in the same direction, from controller to termination. Figures 1–1 and 1–2 show the four signal-flow variations.*

6. Using Figures 1–1 or 1–2, choose which variation is like your system under test. Notice that in two of the configurations the probe adapter can be installed in the first or last RIMM socket, whereas in the other two configurations the probe adapter can only be installed in the middle RIMM socket.

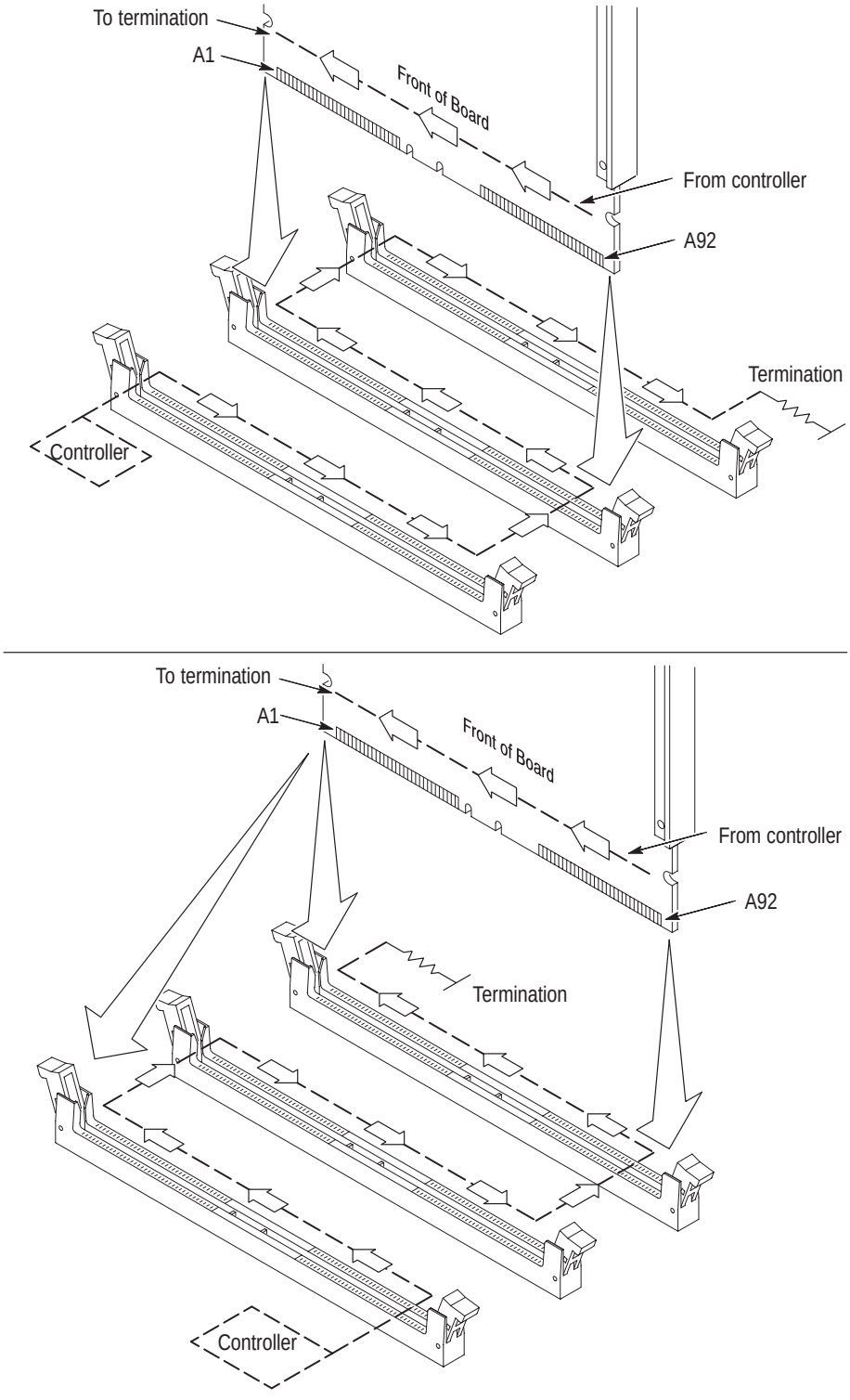


Figure 1–1: Identify slot(s) for probe adapter insertion (front of board)

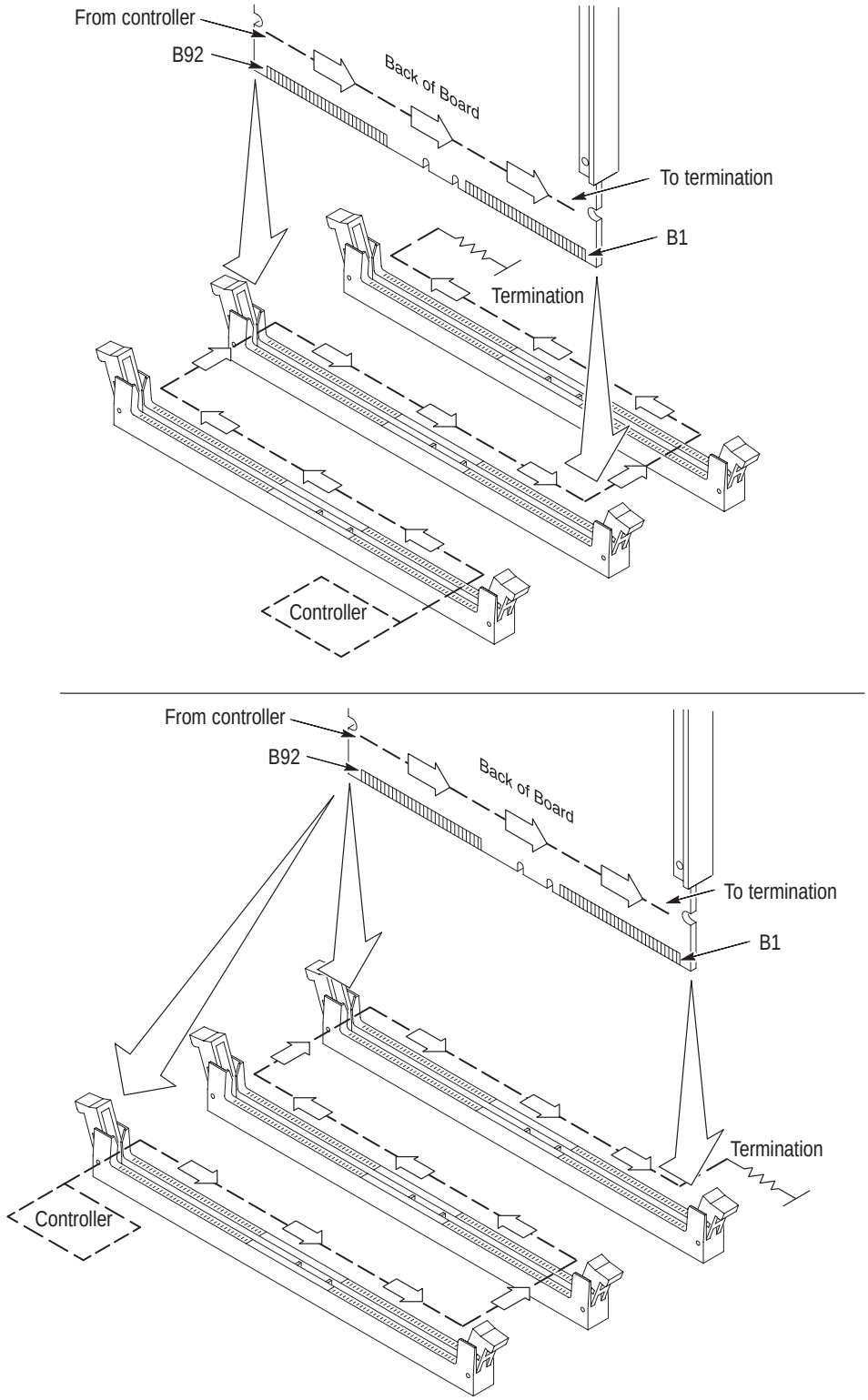


Figure 1–2: Identify slot(s) for probe adapter insertion (back of board)

CAUTION. *To prevent damage to the Rambus Direct RIMM connector on the system under test do not twist or bend the probe adapter while inserting it into the system under test.*

7. Insert the probe adapter into the *Rambus Direct RIMM* connector on the system under test as shown in Figure 1–3.

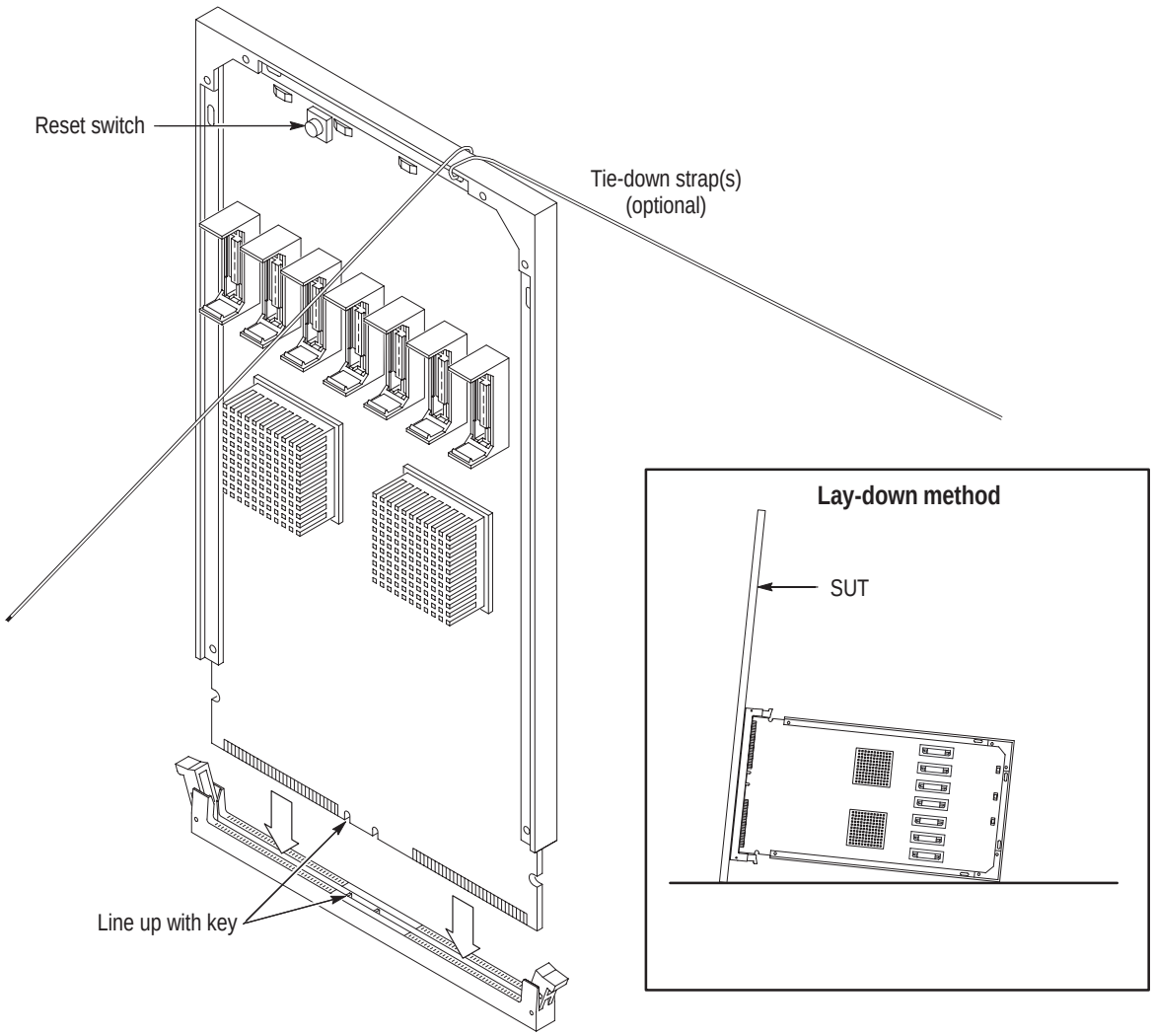


Figure 1–3: Connecting the probe adapter to the system under test.

8. Optional: Attach a tie-down strap(s) through the slot(s) on the probe adapter, and then to the SUT or the benchtop (see Figure 1–3). This step minimizes movement in the Rambus Direct RIMM connector after insertion of the probe adapter.

CAUTION. *To prevent damage to the probe and probe adapter, always position the probe perpendicular to the mating connector and gently connect the probe. Incorrect handling of the P6434 probe while connecting it to the probe adapter can result in damage to the probe or to the mating connector on the probe adapter.*

9. Use the P6434 probes to connect to the Mictor connectors on the Rambus probe adapter. Match the A, C, D and E, probes from the LO module with the corresponding LO_A, LO_C, LO_D and LO_E probe connectors on the probe adapter. Match the A, C, and D probes from the HI module with corresponding HI_A, HI_C, and HI_D probe connections on the probe adapter. Align the pin 1 indicator on the probe label with the pin 1 of the connector on the probe adapter.

The module in the higher-numbered slot is referred to as the slave module, and the module in the lower-numbered slot is referred to as the master module.

10. Position the probe tip perpendicular to the mating connector and gently connect the probe as shown in Figure 1–4.

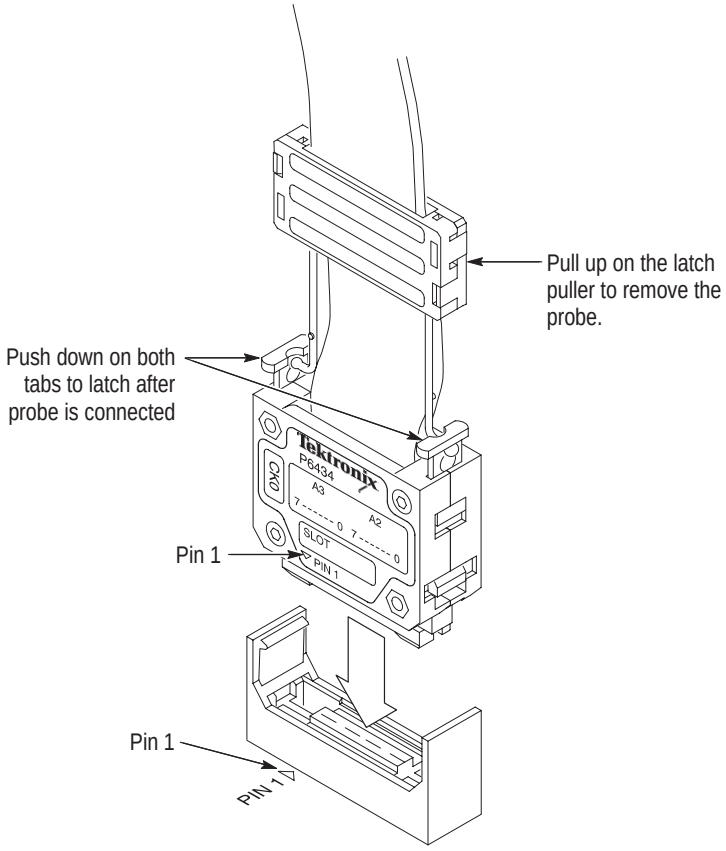


Figure 1–4: Connecting a probe to the connector on the probe adapter

11. When connected, push down on the latch releases on the probe to set the latch.

12. Repeat steps 10 and 11 for the remaining probes.

13. Connect the module ends of the P6434 probes to the corresponding connectors (match label colors) on the logic analyzer. The probe module ends are polarized.

Applying and Removing Power

The power supplies for the TMS 810 Rambus Direct probe adapter are included with this TMS 810 Rambus Direct support package. The power supplies provide +5 volts to the probe adapter.

CAUTION. *To prevent damage to the probe adapter, remove power from the probe adapter whenever you power off the system under test.*

To apply power to the Rambus probe adapter, follow these steps:

CAUTION. *To prevent permanent damage to the probe adapter, use the +5 V power supplies provided by Tektronix. Do not mistake similar power supplies for the +5 V power supplies.*

1. Connect the +5 V power supplies to the jacks on the probe adapter. Figure 1–5 shows the location of the jacks on the probe adapter board.

CAUTION. *To prevent damage to the system under test, apply power to the probe adapter before applying power to your system under test.*

2. Plug the power supplies for the probe adapter into an electrical outlet. When power is present on the probe adapter, an LED lights near each power jack.

3. Power on the system under test.

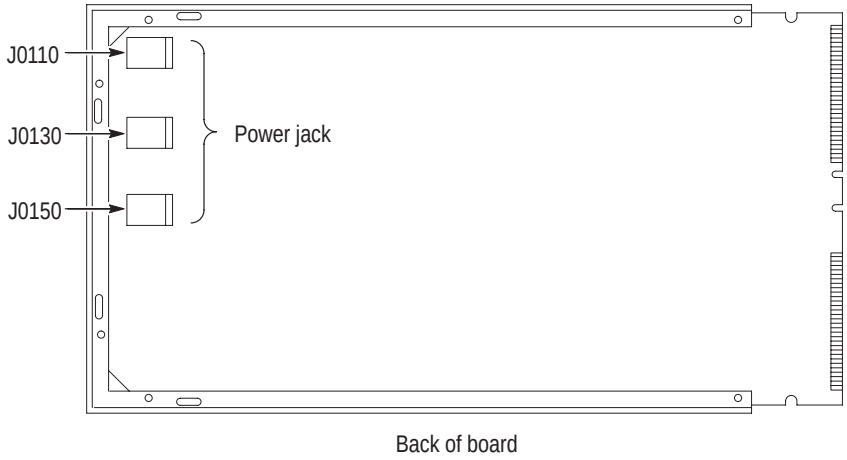


Figure 1–5: Location of the power jacks

To remove power from the system under test and the probe adapter, follow these steps:

CAUTION. *To prevent damage to the system under test, remove power from your system under test before removing power from the probe adapter.*

1. Power off the system under test.
2. Unplug the power supplies from the probe adapter from the electrical outlet.

Reset Switch

You can issue a reset by pressing the button on top of the reset switch (see Figure 1–6 for location).

***NOTE**. If either of the following conditions occur you must reset the probe adapter or you will acquire incorrect data: any time the Rambus clock has been stopped and restarted or power to the SUT is turned off and on again. Pressing the Reset button has no effect on the SUT.*

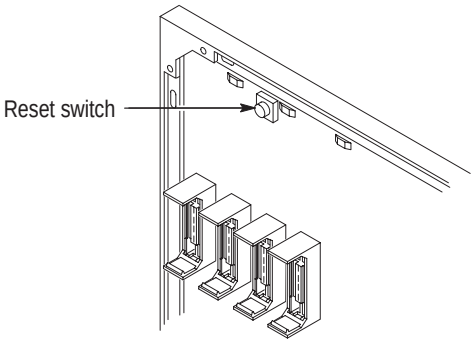


Figure 1–6: Location of the Reset switch

Removing the Probe Adapter from the SUT

To remove the Rambus Direct probe adapter from the system under test, follow these steps:

***CAUTION.** To prevent static damage, handle the components only in a static-free environment. Static discharge can damage the Rambus Direct RIMM module, the probe adapter, the probes, and the logic analyzer module.*

Always wear a grounding wrist strap, heel strap or similar device while handling the Rambus Direct module and probe adapter.

1. Power off your system under test and the probe adapter. It is not necessary to power off the logic analyzer.
2. Disconnect the +5 V power supplies from the jacks on the probe adapter.
3. Disconnect the probes from the probe adapter assembly. Use the latch puller to release the probes.
4. Release the tie-downs from your system under test or bench top.

CAUTION. *To prevent damage to the Rambus Direct RIMM connectors carefully perform step 5.*

5. Disconnect the probe adapter from your system under test using the latch release levers on the Rambus Direct RIMM socket.
6. Place the probe adapter back into the protective bag it was shipped in.
7. Reinstall the Rambus Direct RIMM module into your system under test.

Channel Assignments

Channel assignments listed in Tables 1–2 through Table 1–29 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are listed starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- The module in the higher-numbered slot is referred to as the HI module and the module in the lower-numbered slot is referred to as the LO module.

  The portable logic analyzer has the lower numbered slot on the top and the benchtop logic analyzer has the lower numbered slot on the left.

The following are Rambus channel groups:

ROP	MA	P1
DRA	MB	PA
BRA	COL	PB
RA	D0[63:32]	SIO
ROW	D0[31:00]	Misc
COP	D1[63:32]	
DCA	D1[31:00]	
BCA	DA[63:32]	
CA	DA[31:00]	
XOP	DB[63:32]	
DXA	DB[31:00]	
BXA	P0	

Table 1–1 lists the Rambus signals for each channel of the Row Opcode group. By default the ROP channel group assignments are displayed as symbols. The symbol table file name is Rambus_ROP.

Table 1–1: Row Opcode channel group assignments

Bit order	Rambus signal name
12	ROW–VALID
11	AV
10	ROP10
9	ROP9
8	ROP8
7	ROP7

Table 1–1: Row Opcode channel group assignments (Cont.)

Bit order	Rambus signal name
6	ROP6
5	ROP5
4	ROP4
3	ROP3
2	ROP2
1	ROP1
0	ROP0

Table 1–2 lists the Rambus signals for each channel of the Device Row Address group. By default the DRA channel group assignments are displayed as symbols. The symbol table file name is Rambus_DRA.

Table 1–2: Device Row Address channel group assignments

Bit order	Rambus signal name
6	ROW–VALID
5	DR4T
4	DR4F
3	DR3
2	DR2
1	DR1
0	DR0

Table 1–3 lists the Rambus signals for each channel the Bank Row Address group. By default the BRA channel group assignments are displayed as hexadecimal.

Table 1–3: Bank Row Address channel group assignments

Bit order	Rambus signal name
5	BR5
4	BR4
3	BR3

Table 1–3: Bank Row Address channel group assignments (Cont.)

Bit order	Rambus signal name
2	BR2
1	BR1
0	BR0

Table 1–4 lists the Rambus signals for each channel the Row Address group. By default the RA channel group assignments are displayed as hexadecimal.

Table 1–4: Row Address channel group assignments

Bit order	Rambus signal name
10	R10
9	R9
8	R8
7	R7
6	R6
5	R5
4	R4
3	R3
2	R2
1	R1
0	R0

Table 1–5 lists the Rambus signals for each channel of the Row Packet group. By default the ROW channel group assignments are displayed as symbols. The symbol table file name is Rambus_ROW.

Table 1–5: Row Packet channel group assignments

Bit order	Rambus signal name
2	ROW–VALID
1	ROW–TMG1
0	ROW–TMG0

Table 1–6 lists the Rambus signals for each channel of the Column Opcode group. By default the COP channel group assignments are displayed as symbols. The symbol table file name is Rambus_COP.

Table 1–6: Column Opcode channel group assignments

Bit order	Rambus signal name
5	COL–VALID
4	S
3	COP3
2	COP2
1	COP1
0	COP0

Table 1–7 lists the Rambus signals for each channel of the Device Column Address group. By default the DCA channel group assignments are displayed as hexadecimal.

Table 1–7: Device Column Address channel group assignments

Bit order	Rambus signal name
4	DC4
3	DC3
2	DC2
1	DC1
0	DC0

Table 1–8 lists the Rambus signals for each channel of the Bank Column Address group. By default the BCA channel group assignments are displayed as hexadecimal.

Table 1–8: Bank Column Address channel group assignments

Bit order	Rambus signal name
5	BC5
4	BC4

Table 1–8: Bank Column Address channel group assignments (Cont.)

Bit order	Rambus signal name
3	BC3
2	BC2
1	BC1
0	BC0

Table 1–9 lists the Rambus signals for each channel of the Column Address group. By default the CA channel group assignments are displayed as hexadecimal.

Table 1–9: Column Address channel group assignments

Bit order	Rambus signal name
6	C6
5	C5
4	C4
3	C3
2	C2
1	C1
0	C0

Table 1–10 lists the Rambus signals for each channel of the XOP Opcode group. By default the XOP channel group assignments are displayed as symbols. The symbol table file name is Rambus_XOP.

Table 1–10: XOP Opcode channel group assignments

Bit order	Rambus signal name
7	COL-VALID
6	S
5	M
4	XOP4
3	XOP3
2	XOP2

Table 1–10: XOP Opcode channel group assignments (Cont.)

Bit order	Rambus signal name
1	XOP1
0	XOP0

Table 1–11 lists the Rambus signals for each channel of the Device XOP Address group. By default the DXA channel group assignments are displayed as hexadecimal.

Table 1–11: Device XOP Address channel group assignments

Bit order	Rambus signal name
4	DX4
3	DX3
2	DX2
1	DX1
0	DX0

Table 1–12 lists the Rambus signals for each channel of the Bank XOP Address group. By default the BXA channel group assignments are displayed as hexadecimal.

Table 1–12: Bank XOP Address channel group assignments

Bit order	Rambus signal name
5	BX5
4	BX4
3	BX3
2	BX2
1	BX1
0	BX0

Table 1–13 lists the Rambus signals for each channel of Mask A group. By default the MA channel group assignments are displayed in hexadecimal.

Table 1–13: Mask A channel group assignments

Bit order	Rambus signal name
7	MA7
6	MA6
5	MA5
4	MA4
3	MA3
2	MA2
1	MA1
0	MA0

Table 1–14 lists the Rambus signals for each channel of Mask B group. By default the MB channel group assignment is displayed in hexadecimal.

Table 1–14: Mask B channel group assignments

Bit order	Rambus signal name
7	MB7
6	MB6
5	MB5
4	MB4
3	MB3
2	MB2
1	MB1
0	MB0

Table 1–15 lists the Rambus signals for each channel of the Column Packet group. By default the COL channel group assignments are displayed as symbols. The symbol table file name is Rambus_COL.

Table 1–15: Column Packet channel group assignments

Bit order	Rambus signal name
2	COL–VALID
1	COL–TMG1
0	COL–TMG0

Table 1–16 lists the Rambus signals for each channel of the D0[63:32] group. By default the D0[63:32] channel group assignment is displayed in hexadecimal. This channel group assignment matches the Front Side Bus byte order.

Table 1–16: D0[63:32] channel group assignments

Bit order	Rambus signal name
31	DB34
30	DB33
29	DB32
28	DB31
27	DB30
26	DB29
25	DB28
24	DB27
23	DA34
22	DA33
21	DA32
20	DA31
19	DA30
18	DA29
17	DA28
16	DA27
15	DB25
14	DB24

Table 1–16: D0[63:32] channel group assignments (Cont.)

Bit order	Rambus signal name
13	DB23
12	DB22
11	DB21
10	DB20
9	DB19
8	DB18
7	DA25
6	DA24
5	DA23
4	DA22
3	DA21
2	DA20
1	DA19
0	DA18

Table 1–17 lists the Rambus signals for each channel of the D0[31:00] group. By default the D0[31:00] channel group assignments are displayed in hexadecimal. This channel group assignment matches the Front Side Bus byte order.

Table 1–17: D0[31:00] channel group assignments

Bit order	Rambus signal name
31	DB16
30	DB15
29	DB14
28	DB13
27	DB12
26	DB11
25	DB10
24	DB9
23	DA16
22	DA15

Table 1–17: D0[31:00] channel group assignments (Cont.)

Bit order	Rambus signal name
21	DA14
20	DA13
19	DA12
18	DA11
17	DA10
16	DA9
15	DB7
14	DB6
13	DB6
12	DB4
11	DB3
10	DB2
9	DB1
8	DB0
7	DA7
6	DA6
5	DA5
4	DA4
3	DA3
2	DA2
1	DA1
0	DA0

Table 1–18 lists the Rambus signals for each channel of the D1[63:32] group. By default the D1[63:32] channel group assignment is displayed in hexadecimal. This channel group assignment matches the Front Side Bus byte order.

Table 1–18: D1[63:32] channel group assignments

Bit order	Rambus signal name
31	DB70
30	DB69

Table 1–18: D1[63:32] channel group assignments (Cont.)

Bit order	Rambus signal name
29	DB68
28	DB67
27	DB66
26	DB65
25	DB64
24	DB63
23	DA70
22	DA69
21	DA68
20	DA67
19	DA66
18	DA65
17	DA64
16	DA63
15	DB61
14	DB60
13	DB59
12	DB58
11	DB57
10	DB56
9	DB55
8	DB54
7	DA61
6	DA60
5	DA59
4	DA58
3	DA57
2	DA56
1	DA55
0	DA54

Table 1–19 lists the Rambus signals for each channel of the D1[31:00] group. By default the D1[31:00] channel group assignment is displayed in hexadecimal. This channel group assignment matches the Front Side Bus byte order.

Table 1–19: D1[31:00] channel group assignments

Bit order	Rambus signal name
31	DB52
30	DB51
29	DB50
28	DB49
27	DB48
26	DB47
25	DB46
24	DB45
23	DA52
22	DA51
21	DA50
20	DA49
19	DA48
18	DA47
17	DA46
16	DA45
15	DB43
14	DB42
13	DB41
12	DB40
11	DB39
10	DB38
9	DB37
8	DB36
7	DA43
6	DA42
5	DA41
4	DA40
3	DA39
2	DA38

Table 1–19: D1[31:00] channel group assignments (Cont.)

Bit order	Rambus signal name
1	DA37
0	DA36

Table 1–20 lists the Rambus signals for each channel of the DA[63:32] group. By default the DA[63:32] channel group assignment is displayed in hexadecimal. This channel group assignment matches the Rambus transmission byte order.

Table 1–20: DA[63:32] channel group assignments

Bit order	Rambus signal name
31	DA70
30	DA69
29	DA68
28	DA67
27	DA66
26	DA65
25	DA64
24	DA63
23	DA61
22	DA60
21	DA59
20	DA58
19	DA57
18	DA56
17	DA55
16	DA54
15	DA52
14	DA51
13	DA50
12	DA49
11	DA48
10	DA47
9	DA46

Table 1–20: DA[63:32] channel group assignments (Cont.)

Bit order	Rambus signal name
8	DA45
7	DA43
6	DA42
5	DA41
4	DA40
3	DA39
2	DA38
1	DA37
0	DA36

Table 1–21 lists the Rambus signals for each channel of the DA[31:00] group. By default the DA[31:00] channel group assignment is displayed in hexadecimal. This channel group assignment matches the Rambus Transmission byte order.

Table 1–21: DA[31:00] channel group assignments

Bit order	Rambus signal name
31	DA34
30	DA33
29	DA32
28	DA31
27	DA30
26	DA29
25	DA28
24	DA27
23	DA25
22	DA24
21	DA23
20	DA22
19	DA21
18	DA20
17	DA19
16	DA18

Table 1–21: DA[31:00] channel group assignments (Cont.)

Bit order	Rambus signal name
15	DA16
14	DA15
13	DA14
12	DA13
11	DA12
10	DA11
9	DA10
8	DA9
7	DA7
6	DA6
5	DA5
4	DA4
3	DA3
2	DA2
1	DA1
0	DA0

Table 1–22 lists the Rambus signals for each channel of the DB[63:32] group. By default the DB[63:32] channel group assignments are displayed in hexadecimal. This channel group assignment matches the Rambus Transmission order.

Table 1–22: DB[63:32] channel group assignments

Bit order	Rambus signal name
31	DB70
30	DB69
29	DB68
28	DB67
27	DB66
26	DB65
25	DB64
24	DB63

Table 1–22: DB[63:32] channel group assignments (Cont.)

Bit order	Rambus signal name
23	DB61
22	DB60
21	DB59
20	DB58
19	DB57
18	DB56
17	DB55
16	DB54
15	DB52
14	DB51
13	DB50
12	DB49
11	DB48
10	DB47
9	DB46
8	DB45
7	DA43
6	DA42
5	DA41
4	DA40
3	DA39
2	DA38
1	DA37
0	DA36

Table 1–23 lists the Rambus signals for each channel of the DB[31:00] group. By default the DB[31:00] channel group assignment is displayed in hexadecimal. This channel group assignment matches the Rambus Transmission order.

Table 1–23: DB[31:00] channel group assignments

Bit order	Rambus signal name
31	DB34
30	DB33
29	DB32
28	DB31
27	DB30
26	DB29
25	DB28
24	DB27
23	DB25
22	DB24
21	DB23
20	DB22
19	DB21
18	DB20
17	DB19
16	DB18
15	DB16
14	DB15
13	DB14
12	DB13
11	DB12
10	DB11
9	DB10
8	DB9
7	DB7
6	DB6
5	DB5
4	DB4
3	DB3
2	DB2

Table 1–23: DB[31:00] channel group assignments (Cont.)

Bit order	Rambus signal name
1	DB1
0	DB0

Table 1–24 lists the Rambus signals for each channel of the P0 group. By default the P0 channel group assignment is not displayed. This channel group assignment matches the Front Side Bus byte order.

Table 1–24: P0 channel group assignments

Bit order	Rambus signal name
7	DB35
6	DA35
5	DB26
4	DA26
3	DB17
2	DA17
1	DB8
0	DA8

Table 1–25 lists the Rambus signals for each channel of the P1 group. By default the P1 channel group assignment is not displayed. This channel group assignment matches the Front Side Bus byte order.

Table 1–25: P1 channel group assignments

Bit order	Rambus signal name
7	DB71
6	DA71
5	DB62
4	DA62
3	DB53
2	DA53
1	DB44
0	DA44

Table 1–26 lists the Rambus signals for each channel of the PA group. By default the PA channel group assignment is not displayed. This channel group assignment matches the Rambus Transmission order.

Table 1–26: PA channel group assignments

Bit order	Rambus signal name
7	DA71
6	DA62
5	DA53
4	DA44
3	DA35
2	DA26
1	DA17
0	DA8

Table 1–27 lists the Rambus signals for each channel of the PB group. By default the PB channel group assignment is not displayed. This channel group assignment matches the Rambus Transmission order.

Table 1–27: PB channel group assignments

Bit order	Rambus signal name
7	DB71
6	DB62
5	DB53
4	DB44
3	DB35
2	DB26
1	DB17
0	DB8

Table 1–28 lists the Rambus signals for each channel of the SIO group. By default the SIO channel group assignment is displayed as symbols. The symbol table file name is Rambus_SIO.

Table 1–28: SIO channel group assignments

Bit order	Rambus signal name
1	SIO-1
0	SIO-0

Table 1–29 lists the Rambus signals for each channel of the Misc group. By default the Misc channel group assignment is not displayed.

Table 1–29: Misc channel group assignments

Bit order	Rambus signal name
1	CLK-X1
0	CLK-X0

Table 1–30 lists signals not required for disassembly.

Table 1–30: Signals not required for disassembly.

Rambus signal name	AUX pin number
GND	1
SIO[1]	2
SCK[1]	3
CMD[1]	4

1 The SIO, SCK, and CMD signals are not acquired as Control Register Transactions, but are acquired as a part of the Power State Transitions. You can use the AUX connector to probe these signals.

The following is a list of signals that are not available on the probe adapter. Any of these signals can be probed from the bottom of the system under test.

CFM[1]	SCL	SA1	V_{DD}
CFMN[1]	SWP	SA2	V_{REF}[2]
CTM	SDA	SV_{DD}	
CTMN	SA0	V_{CMOS}	

1 The CFM and CFMN signals are used by the probe adapter to derive the 100 MHz acquisition clock, but are not otherwise available on the probe adapter.

2 The V_{REF} signal is used by the probe adapter, but is not otherwise available on the probe adapter.

The following is a list of extra acquisition channels that are not attached to the probe adapter. Extra acquisition channels are only available if the second module is a 136-channel module.

HI_E3:7-0

HI_E2:7-0

HI_E1:7-0

HI_E0:7-0

HI_Qual:2

HI_Qual:3

Packet Definitions

Tables 1–31 through 1–34 list packet definitions.

Table 1–31: Row packets

		ROWA packet definition				ROWR packet definition			
			DRA group	BRA group	RA group		DRA group	BRA group	ROP group
TLA channel number	Signal name	ROWA packet	Device row address	Bank row address	Row address	ROWR packet	Device row address	Bank row address	Row Opcode
LO_D1:5	ROW2-T0	DR4T	DR4T			DR4T	DR4T		
LO_D1:6	ROW1-T0	DR4F	DR4F			DR4F	DR4F		
LO_D1:7	ROW0-T0	DR3	DR3			DR3	DR3		
HI_D1:5	ROW2-TI	DR2	DR2			DR2	DR2		
HI_D1:6	ROW1-TI	DR1	DR1			DR1	DR1		
HI_D1:7	ROW0-TI	DR0	DR0			DR0	DR0		
LO_D1:2	ROW2-T2	BR0		BR0		BR0		BR0	
LO_D1:3	ROW1-T2	BR1		BR1		BR1		BR1	
LO_D1:4	ROW0-T2	BR2		BR2		BR2		BR2	
HI_D1:2	ROW2-T3	BR3		BR3		BR3		BR3	
HI_D1:3	ROW1-T3	BR4		BR4		BR4		BR4	
HI_D1:4	ROW0-T3	BR5		BR5		BR5		BR5	
LO_D0:7	ROW2-T4	R10			R10	ROP10			ROP10
LO_D1:0	ROW1-T4	R9			R9	ROP9			ROP9
LO_D1:1	ROW0-T4	AV=1			AV=1	AV=0			AV=0
HI_D0:7	ROW2-T5	R8			R8	ROP8			ROP8
HI_D1:0	ROW1-T5	R7			R7	ROP7			ROP7
HI_D1:1	ROW0-T5	R6			R6	ROP6			ROP6
LO_D0:4	ROW2-T6	R5			R5	ROP5			ROP5
LO_D0:5	ROW1-T6	R4			R4	ROP4			ROP4
LO_D0:6	ROW0-T6	R3			R3	ROP3			ROP3
HI_D0:4	ROW2-T7	R2			R2	ROP2			ROP2
HI_D0:5	ROW1-T7	R1			R1	ROP1			ROP1
HI_D0:6	ROW0-T7	R0			R0	ROP0			ROP0

Table 1–32: Column packets

Group name ▶		COLC packet definition					COLX packet definition				COLM packet definition		
			DCA	BCA	CA	COP		DXA	BXA	XOP		MA	MB
TLA channel number	Siganl name	COLC packet	Device column address	Bank column address	Column address	Column Opcode	COLX packet	Device XOP address	Bank XOP address	XOP Opcode	COLM packet	Mask A byte mask	Mask B byte mask
LO_D2:0	COL4-T0	DC4	DC4										
LO_D0:0	COL3-T0	DC3	DC3										
LO_D0:1	COL2-T0	DC2	DC2										
LO_D0:2	COL1-T0	DC1	DC1										
LO_D0:3	COL0-T0	DC0	DC0										
HI_D2:0	COL4-T1	S=1	S=1	S=1	S=1	S=1	S=1	S=1	S=1	S=1	S=1	S=1	S=1
HI_D0:0	COL3-T1						M=0	M=0	M=0	M=0	M=1	M=1	M=1
HI_D0:1	COL2-T1	COP1				COP1							
HI_D0:2	COL1-T1	COP0				COP0							
HI_D0:3	COL0-T1	COP2				COP2							
LO_D2:5	COL4-T2						DX4	DX4			MA7	MA7	
LO_D2:4	COL3-T2						DX3	DX3			MA6	MA6	
LO_D2:3	COL2-T2						DX2	DX2			MB7		MB7
LO_D2:2	COL1-T2						DX1	DX1			MB6		MB6
LO_D2:1	COL0-T2						DX0	DX0			MB5		MB5
HI_D2:5	COL4-T3						XOP4			XOP4	MA5	MA5	
HI_D2:4	COL3-T3						XOP3			XOP3	MA4	MA4	
HI_D2:3	COL2-T3						XOP2			XOP2	MB4		MB4
HI_D2:2	COL1-T3						XOP1			XOP0	MB3		MB3
HI_D2:1	COL0-T3						XOP0			XOP1	MB2		MB2
LO_D3:2	COL4-T4						BX5		BX5		MA3	MA3	
LO_D3:1	COL3-T4						BX4		BX4		MA2	MA2	
LO_D3:0	COL2-T4						BX3		BX3		MB1		MB1
LO_D2:7	COL1-T4						BX2		BX2		MB0		MB0
LO_D2:6	COL0-T4	COP3				COP3							
HI_D3:2	COL4-T5						BX1		BX1		MA1	MA1	
HI_D3:1	COL3-T5						BX2		BX0		MA0	MA0	
HI_D3:0	COL2-T5	BC5		BC5									
HI_D2:7	COL1-T5	BC4		BC4									
HI_D2:6	COL0-T5	BC3		BC3									
LO_D3:7	COL4-T6	C6			C6								

Table 1–32: Column packets (cont.)

Group name ▶		COLC packet definition					COLX packet definition				COLM packet definition		
			DCA	BCA	CA	COP		DXA	BXA	XOP		MA	MB
TLA channel number	Siganl name	COLC packet	Device column address	Bank column address	Column address	Column Opcode	COLX packet	Device XOP address	Bank XOP address	XOP Opcode	COLM packet	Mask A byte mask	Mask B byte mask
LO_D3:6	COL3-T6	C5			C5								
LO_D3:5	COL2-T6	BC2		BC2									
LO_D3:4	COL1-T6	BC1		BC1									
LO_D3:3	COL0-T6	BC0		BC0									
HI_D3:7	COL4-T7	C4			C4								
HI_D3:6	COL3-T7	C3			C3								
HI_D3:5	COL2-T7	C2			C2								
HI_D3:4	COL1-T7	C1			C1								
HI_D3:3	COL0-T7	C0			C0								

Table 1–33: Write data A packets

Group name		Data A packet definition						
			D0[63:32] group	D0[31:00] group	D1[63:32] group	D1[31:00] group	P0 group	P1 group
TLA Channel number	Signal name	Data A packet	D0[63:32]	D0[31:00]	D1[63:32]	D1[31:00]	P0	P1
LO_E1:7	DQA8-T0	DA8					DA8	
LO_C1:0	DQA7-T0	DA7		DA7				
LO_C1:1	DQA6-T0	DA6		DA6				
LO_C1:2	DQA5-T0	DA5		DA5				
LO_C1:3	DQA4-T0	DA4		DA4				
LO_C1:4	DQA3-T0	DA3		DA3				
LO_C1:5	DQA2-T0	DA2		DA2				
LO_C1:6	DQA1-T0	DA1		DA1				
LO_C1:7	DQA0-T0	DA0		DA0				
HI_Q:0	DQA8-T1	DA17					DA17	
HI_C1:0	DQA7-T1	DA16		DA16				
HI_C1:1	DQA6-T1	DA15		DA15				
HI_C1:2	DQA5-T1	DA14		DA14				
HI_C1:3	DQA4-T1	DA13		DA13				

Table 1–33: Write data A packets (cont.)

Group name		Data A packet definition						
			D0[63:32] group	D0[31:00] group	D1[63:32] group	D1[31:00] group	P0 group	P1 group
TLA Channel number	Signal name	Data A packet	D0[63:32]	D0[31:00]	D1[63:32]	D1[31:00]	P0	P1
HI_C1:4	DQA3-T1	DA12		DA12				
HI_C1:5	DQA2-T1	DA11		DA11				
HI_C1:6	DQA1-T1	DA10		DA10				
HI_C1:7	DQA0-T1	DA9		DA9				
LO_E1:6	DQA8-T2	DA26					DA26	
LO_C0:0	DQA7-T2	DA25	DA25					
LO_C0:1	DQA6-T2	DA24	DA24					
LO_C0:2	DQA5-T2	DA23	DA23					
LO_C0:3	DQA4-T2	DA22	DA22					
LO_C0:4	DQA3-T2	DA21	DA21					
LO_C0:5	DQA2-T2	DA20	DA20					
LO_C0:6	DQA1-T2	DA19	DA19					
LO_C0:7	DQA0-T2	DA18	DA18					
HI_Q:1	DQA8-T3	DA35					DA35	
HI_C0:0	DQA7-T3	DA34	DA34					
HI_C0:1	DQA6-T3	DA33	DA33					
HI_C0:2	DQA5-T3	DA32	DA32					
HI_C0:3	DQA4-T3	DA31	DA31					
HI_C0:4	DQA3-T3	DA30	DA30					
HI_C0:5	DQA2-T3	DA29	DA29					
HI_C0:6	DQA1-T3	DA28	DA28					
HI_C0:7	DQA0-T3	DA27	DA27					
LO_E1:5	DQA8-T4	DA44						DA44
LO_C2:7	DQA7-T4	DA43				DA43		
LO_C2:6	DQA6-T4	DA42				DA42		
LO_C2:5	DQA5-T4	DA41				DA41		
LO_C2:4	DQA4-T4	DA40				DA40		
LO_C2:3	DQA3-T4	DA39				DA39		
LO_C2:2	DQA2-T4	DA38				DA38		
LO_C2:1	DQA1-T4	DA37				DA37		
LO_C2:0	DQA0-T4	DA36				DA36		

Table 1–33: Write data A packets (cont.)

Group name		Data A packet definition						
			D0[63:32] group	D0[31:00] group	D1[63:32] group	D1[31:00] group	P0 group	P1 group
TLA Channel number	Signal name	Data A packet	D0[63:32]	D0[31:00]	D1[63:32]	D1[31:00]	P0	P1
HI_CLK:3	DQA8-T5	DA53						DA53
HI_C2:7	DQA7-T5	DA52				DA52		
HI_C2:6	DQA6-T5	DA51				DA51		
HI_C2:5	DQA5-T5	DA50				DA50		
HI_C2:4	DQA4-T5	DA49				DA49		
HI_C2:3	DQA3-T5	DA48				DA48		
HI_C2:2	DQA2-T5	DA47				DA47		
HI_C2:1	DQA1-T5	DA46				DA46		
HI_C2:0	DQA0-T5	DA45				DA45		
LO_E1:4	DQA8-T6	DA62						DA62
LO_C3:7	DQA7-T6	DA61			DA61			
LO_C3:6	DQA6-T6	DA60			DA60			
LO_C3:5	DQA5-T6	DA59			DA59			
LO_C3:4	DQA4-T6	DA58			DA58			
LO_C3:3	DQA3-T6	DA57			DA57			
LO_C3:2	DQA2-T6	DA56			DA56			
LO_C3:1	DQA1-T6	DA55			DA55			
LO_C3:0	DQA0-T6	DA54			DA54			
HI_CLK:1	DQA8-T7	DA71						DA71
HI_C3:7	DQA7-T7	DA70			DA70			
HI_C3:6	DQA6-T7	DA69			DA69			
HI_C3:5	DQA5-T7	DA68			DA68			
HI_C3:4	DQA4-T7	DA67			DA67			
HI_C3:3	DQA3-T7	DA66			DA66			
HI_C3:2	DQA2-T7	DA65			DA65			
HI_C3:1	DQA1-T7	DA64			DA64			
HI_C3:0	DQA0-T7	DA63			DA63			

Table 1–34: Write Data B Packets

Group name		Data A packet definition						
			D0[63:32] group	D0[31:00] group	D1[63:32] group	D1[31:00] group	P0 group	P1 group
TLA Channel number	Signal name	Data A packet	D0[63:32]	D0[31:00]	D1[63:32]	D1[31:00]	P0	P1
LO_E1:3	DQB8-T0	DB8					DB8	
LO_A1:0	DQB7-T0	DB7		DB7				
LO_A1:1	DQB6-T0	DB6		DB6				
LO_A1:2	DQB5-T0	DB5		DB5				
LO_A1:3	DQB4-T0	DB4		DB4				
LO_A1:4	DQB3-T0	DB3		DB3				
LO_A1:5	DQB2-T0	DB2		DB2				
LO_A1:6	DQB1-T0	DB1		DB1				
LO_A1:7	DQB0-T0	DB0		DB0				
LO_E3:4	DQB8-T1	DB17					DB17	
HI_A1:0	DQB7-T1	DB16		DB16				
HI_A1:1	DQB6-T1	DB15		DB15				
HI_A1:2	DQB5-T1	DB14		DB14				
HI_A1:3	DQB4-T1	DB13		DB13				
HI_A1:4	DQB3-T1	DB12		DB12				
HI_A1:5	DQB2-T1	DB11		DB11				
HI_A1:6	DQB1-T1	DB10		DB10				
HI_A1:7	DQB0-T1	DB9		DB9				
LO_E1:2	DQB8-T2	DB26					DB26	
LO_A0:0	DQB7-T2	DB25	DB25					
LO_A0:1	DQB6-T2	DB24	DB24					
LO_A0:2	DQB5-T2	DB23	DB23					
LO_A0:3	DQB4-T2	DB22	DB22					
LO_A0:4	DQB3-T2	DB21	DB21					
LO_A0:5	DQB2-T2	DB20	DB20					
LO_A0:6	DQB1-T2	DB19	DB19					
LO_A0:7	DQB0-T2	DB18	DB18					
LO_E3:5	DQB8-T3	DB35					DB35	
HI_A0:0	DQB7-T3	DB34	DB34					
HI_A0:1	DQB6-T3	DB33	DB33					
HI_A0:2	DQB5-T3	DB32	DB32					

Table 1–34: Write Data B Packets (cont.)

Group name		Data A packet definition						
			D0[63:32] group	D0[31:00] group	D1[63:32] group	D1[31:00] group	P0 group	P1 group
TLA Channel number	Signal name	Data A packet	D0[63:32]	D0[31:00]	D1[63:32]	D1[31:00]	P0	P1
HI_A0:3	DQB4-T3	DB31	DB31					
HI_A0:4	DQB3-T3	DB30	DB30					
HI_A0:5	DQB2-T3	DB29	DB29					
HI_A0:6	DQB1-T3	DB28	DB28					
HI_A0:7	DQB0-T3	DB27	DB27					
LO_E1:1	DQB8-T4	DB44						DB44
LO_A2:7	DQB7-T4	DB43				DB43		
LO_A2:6	DQB6-T4	DB42				DB42		
LO_A2:5	DQB5-T4	DB41				DB41		
LO_A2:4	DQB4-T4	DB40				DB40		
LO_A2:3	DQB3-T4	DB39				DB39		
LO_A2:2	DQB2-T4	DB38				DB38		
LO_A2:1	DQB1-T4	DB37				DB37		
LO_A2:0	DQB0-T4	DB36				DB36		
HI–E3:6	DQB8-T5	DB53						DB53
HI_A2:7	DQB7-T5	DB52				DB52		
HI_A2:6	DQB6-T5	DB51				DB51		
HI_A2:5	DQB5-T5	DB50				DB50		
HI_A2:4	DQB4-T5	DB49				DB49		
HI_A2:3	DQB3-T5	DB48				DB48		
HI_A2:2	DQB2-T5	DB47				DB47		
HI_A2:1	DQB1-T5	DB46				DB46		
HI_A2:0	DQB0-T5	DB45				DB45		
LO_E1:0	DQB8-T6	DB62						DB62
LO_A3:7	DQB7-T6	DB61			DB61			
LO_A3:6	DQB6-T6	DB60			DB60			
LO_A3:5	DQB5-T6	DB59			DB59			
LO_A3:4	DQB4-T6	DB58			DB58			
LO_A3:3	DQB3-T6	DB57			DB57			
LO_A3:2	DQB2-T6	DB56			DB56			
LO_A3:1	DQB1-T6	DB55			DB55			

Table 1–34: Write Data B Packets (cont.)

Group name		Data A packet definition						
			D0[63:32] group	D0[31:00] group	D1[63:32] group	D1[31:00] group	P0 group	P1 group
TLA Channel number	Signal name	Data A packet	D0[63:32]	D0[31:00]	D1[63:32]	D1[31:00]	P0	P1
LO_A3:0	DQB0-T6	DB54			DB54			
HI_E3:7	DQB8-T7	DB71						DB71
HI_A3:7	DQB7-T7	DB70			DB70			
HI_A3:6	DQB6-T7	DB69			DB69			
HI_A3:5	DQB5-T7	DB68			DB68			
HI_A3:4	DQB4-T7	DB67			DB67			
HI_A3:3	DQB3-T7	DB66			DB66			
HI_A3:2	DQB2-T7	DB65			DB65			
HI_A3:1	DQB1-T7	DB64			DB64			
HI_A3:0	DQB0-T7	DB63			DB63			

Operating Basics

Setting Up the Support

This section provides information on how to set up the TMS 810 Rambus Direct bus support. The information covers Clocking options, Triggering and Symbol table files.

The information in this section is specific to the operations and functions of the TMS 810 Rambus Direct support on any Tektronix logic analyzer for which it can be purchased.

Before you acquire and display disassembled data, you need to load the support and specify the setups for clocking and triggering as described in the information on basic operations in your online help menu. The support provides default values for each of these setups, but you can change them as needed.

Installing the Support Software

NOTE. *Before you install any software, it is recommended you verify the microprocessor support software is compatible with the logic analyzer software.*

To install the TMS 810 Rambus Direct software on your Tektronix logic analyzer, follow these steps:

1. Insert the floppy disk in the disk drive.
2. Click the Windows Start button, point to Settings, and click Control Panel.
3. In the Control Panel window, double-click Add/Remove Programs.
4. Follow the instructions on the screen for installing the software from the floppy disk.

To remove or uninstall software following the above instructions and select Uninstall. You need to close all windows before you uninstall any software.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the Rambus Direct support are ROP, DRA, BRA, RA, ROW, COP, DCA, BCA, CA, XOP, DXA, BXA, MA, MB, COL, D0[63:32], D0[31:00], D1[63:32], D1[31:00], DA[63:32], DA[31:00], DB[63:32], DB[31:00], P0, P1, PA, PB, and SIO. If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 1–12.

The D0/D1 groups are used for triggering and displaying in the Front Side Bus byte order, whereas, the DA/DB groups are used for triggering and displaying in the Rambus Transmission byte order. This is also true for the P0/P1 and PA/PB parity groups. Following are byte order definitions:

Front Side Bus Byte Order:

	[63:32]				[31:00]			
D0	B3	A3	B2	A2	B1	A1	B0	A0
D1	B7	A7	B6	A6	B5	A5	B4	A4

Rambus Transmission Byte Order:

	[63:32]				[31:00]			
DA	A7	A6	A5	A4	A3	A2	A1	A0
DB	B7	B6	B5	B4	B3	B2	B1	B0

If your CPU bus does not use the same byte order as the Front Side Bus, then you can redefine the byte order of the D0[63:32], D0[31:00], D1[63:32], and D1[31:00] groups to match the byte order of your CPU bus. This is also true for the P0/P1 parity groups. These redefined byte and bit orders can be used in triggering and displaying. You may also want to save this setup for future use.

Clocking

Custom Clocking

A special clocking program is loaded to the module every time you load the Rambus support. This special clocking is called Custom.

When Custom is selected, the Custom Clocking Options menu has the subtitle Rambus Direct Clocking Support added, and the following clocking options are displayed.

Clocking Options

The TMS 810 support offers a bus specific clocking mode for the Rambus Direct bus. This clocking mode is the default selection whenever you load the TMS 810 Rambus Direct support.

The only clocking option provided with the TMS 810 Rambus Direct support package, is the Acquisition Mode. This field contains one selection:

Active Cycles Only

Active Cycles Only refers to all Row and Column Packets, and Write Data Packets. The Active Cycles Only mode must be used for correct acquisition and disassembly.

Triggering

To use a trigger program during bus transactions, you need to set up the Rambus Direct support package to trigger on one or more channel groups. To set up a trigger program, you need to know which channel groups you are including and which channel groups are valid for that trigger program.

NOTE. *If either of the following conditions occur you must reset the probe adapter or you will acquire false trigger data: any time the clock has been stopped and restarted or power to the SUT is turned off and on again (see Figure 1–6 on page 1–10 for the Reset switch location). Pressing the Reset button has no effect on the SUT.*

Avoiding False Triggering

The TMS 810 support package can trigger on invalid channel groups. Before setting up a trigger program, review the following information to reduce false triggering.

When attempting to trigger on a:

- Bank from the **BRA** group, select any device for the **DRA** group or any opcode for the **ROP** group. You do not need to select both a device and an opcode.
- Row from the **RA** group, select the **ACT** opcode for the **ROP** group.
- Device from the **DCA** group, bank from the **BCA** group, or column from the **CA** group, select any opcode for the **COP** group.
- Device from the **DXA** group or bank from the **BXA** group, select any opcode for the **XOP** group.
- Mask from the **MA** group, or mask from the **MB** group, select the **MSK** opcode for the **XOP** group.
- Write data from the **D0[63:32], D0[31:00], D1[63:32], D1[31:00], P0,** or **P1** groups, select the **WR** or **WRA** opcodes for the **COP** group.
- Write data from the **DA[63:32]**, **DA[31:00**], **DB[63:32]**, **DB[31:00]**, **PA**, or **PB** groups, select **WR** or **WRA** opcodes for the **COP** group.
- Do not use both the D0/D1 groups and the DA/DB groups in the same trigger program. This also applies to the P0/P1 groups and PA/PB groups.

Trigger Programs

The TMS 810 Rambus Direct support package provides two trigger programs:

Trig_ROW_COL
Trig_ROW_COL_WD

You can use either trigger program to acquire Rambus Direct bus activity.

To load either trigger program follow these steps:

1. Select Load Trigger from either the LT button or the File pulldown Menu.
2. Browse for the RAMBUS file, and load the trigger program.

   `C:\Program Files\TLA 700\Supports\RAMBUS`

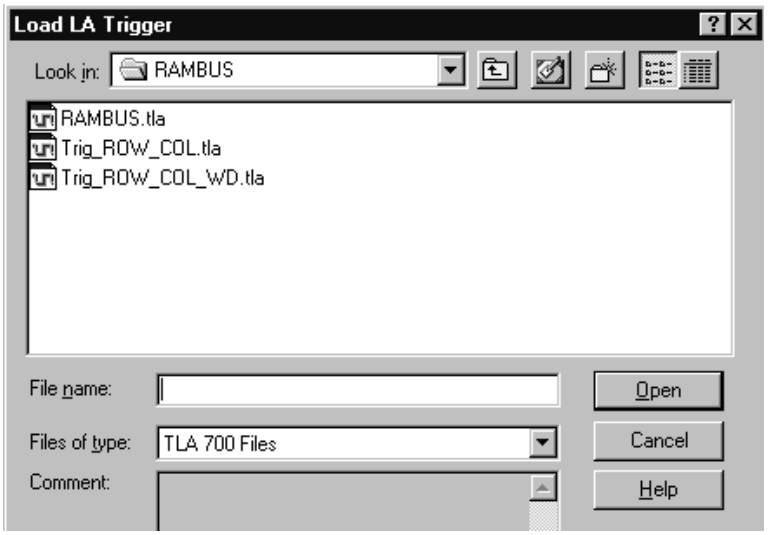


Figure 2–1: Load logic analyzer trigger

Trig_ROW_COL. You need to specify the Row and Column packets, and then enter the value for each group of these packets in the Trig_ROW_COL program.

To setup your trigger program follow these steps:

1. In State 1, Activate Device, Bank, and Row, double click on the only If/Then clause of State 1.

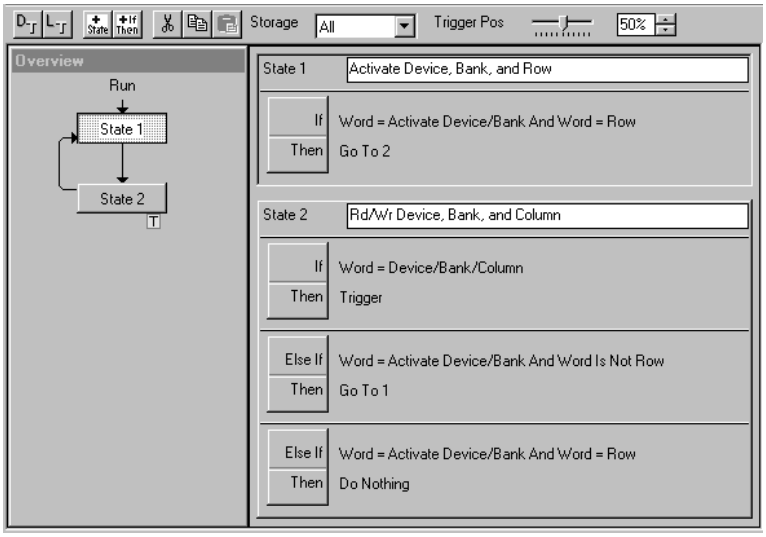


Figure 2–2: Trig_ROW_COL

2. Select Define Word of **Word = Activate Device/Bank**, and then enter the device number in the DRA group and the bank number in the BRA group. Click OK.

NOTE. *In software version 2 you may see the following error message while entering data in various fields:*

```
The selected word definition is in use by a state that contains
more than 4 If/Then clauses.
```

Ignore this message and reenter your data, and the message will disappear. Software releases after version 2 do not have this error.

---

3. Select Define Word of **Word = Row**, and then enter the row number in the RA group. Click OK.

4. In State 2, Rd/Wr Device, Bank, and Column, double click on the first If/Then clause of State 2.

5. Select Define Word of **Word = Device/Bank/Column**, and then select the appropriate opcode in the COP group, and enter the device number in the DCA group, the bank number in the BCA group, and the column number in the CA group. Click OK.

NOTE. *You do not need to change the other two If/Then clauses of State 2.*

---

6. Adjust the trigger position and memory depth, and begin the acquisition of Rambus data.

Trig_ROW_COL_WD. You need to specify the Row packet, the Column packet, and the Write Data packet (equal or not equal), and then, enter a value for each group of these packets in the Trig_ROW_COL_WD program.

To set up your trigger program follow these steps:

1. In State 1, Activate Device, Bank, and Row, double click on the only If/Then clause of State 1.

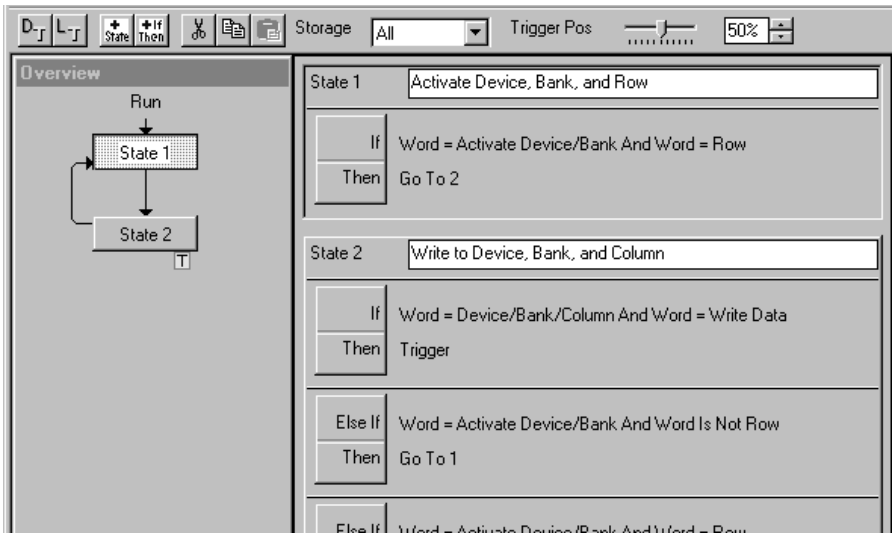


Figure 2–3: Trig_ROW_COL_WD

2. Select Define Word of **Word = Activate Device/Bank**, and then enter the device number in the DRA group and the bank number in BRA group. Click OK.

NOTE. *In software version 2 you may see the following error message while entering data in various fields:*

```
The selected word definition is in use by a state that contains
more than 4 If/Then clauses.
```

Ignore this message and reenter your data, and the message will disappear. Software releases after version 2 do not have this error.

---

3. Select Define Work of **Word = Row**, and then, enter the row number in the RA group. Click OK.

4. In State 2, Write to Device, Bank, and Column, double click on the first If/Then clause of State 2.

5. Select Define Word of **Word = Device/Bank/Column**, and then select the appropriate WR or WRA opcode in the COP group, and enter the device number in the DCA group, the bank number in the BCA group, and the column number in the CA group. Click OK.

6. Select Define Word of **Word = Write Data**, and then enter write data in the D0[63:32], D0[31:00], D1[63:32], and D1[31:00] groups for Front Side Bus byte order, or DA[63:32], DA[31:00], DB[63:32], and DB[31:00] for Rambus Transmission byte order. Do not mix byte orders. Click OK.

   If you want to trigger on any word other than the word you entered, change **Word = Write Data** to **Word Is Not Write Data** and click OK.

NOTE. *You do not need to change the other two If/Then clauses of State 2.*

7. Adjust the trigger position and memory depth, and begin the acquisition of Rambus data.

Trigger Program Operation. Once the specified device, bank, and row has been activated, while the trigger program is waiting for the specified column to be read or written, if the specified row is closed and a different row of the same device and bank is activated, the trigger program will return to waiting for the specified device, bank, and row to be reactivated before it returns to waiting for the specified column to be read or written.

Symbols

The TMS 810 support supplies seven symbol table files. Information on basic operations in your online help menu describes how to use symbolic values for triggering and displaying channel groups symbolically.

Table 2–1 lists the symbol table and channel group names.

Table 2–1: Symbol table information

Symbol table file name	Channel group name
Rambus_DRA	Device Row Address
Rambus_ROP	Row Opcode
Rambus_COP	Column Opcode
Rambus_XOP	XOP Opcode
Rambus_SIO	Serial I/O
Rambus_ROW	Row Packet
Rambus_COL	Column Packet

Table 2–2 lists the name, bit pattern, and description of the symbols in the file Rambus_DRA, in the Device Row Address channel group symbol table.

Table 2–2: Device Row Address group symbol table definitions

Symbol	Rambus_DRA group value ROW-VALID DR4T DR4F DR3 DR2 DR1 DR0	Description
—	0 X X X X X X	No Row Packet
ALL	1 1 1 X X X X	ALL devices (Broadcast)
00	1 0 1 0 0 0 0	Device 0
01	1 0 1 0 0 0 1	Device 1
02	1 0 1 0 0 1 0	Device 2
03	1 0 1 0 0 1 1	Device 3
04	1 0 1 0 1 0 0	Device 4
05	1 0 1 0 1 0 1	Device 5
06	1 0 1 0 1 1 0	Device 6
07	1 0 1 0 1 1 1	Device 7
08	1 0 1 1 0 0 0	Device 8

Table 2–2: Device Row Address group symbol table definitions (cont.)

Symbol	Rambus_DRA group value ROW-VALID DR4T DR4F DR3 DR2 DR1 DR0	Description
09	1 0 1 1 0 0 1	Device 9
0A	1 0 1 1 0 1 0	Device 10
0B	1 0 1 1 0 1 1	Device 11
0C	1 0 1 1 1 0 0	Device 12
0D	1 0 1 1 1 0 1	Device 13
0E	1 0 1 1 1 1 0	Device 14
0F	1 0 1 1 1 1 1	Device 15
10	1 1 0 0 0 0 0	Device 16
11	1 1 0 0 0 0 1	Device 17
12	1 1 0 0 0 1 0	Device 18
13	1 1 0 0 0 1 1	Device 19
14	1 1 0 0 1 0 0	Device 20
15	1 1 0 0 1 0 1	Device 21
16	1 1 0 0 1 1 0	Device 22
17	1 1 0 0 1 1 1	Device 23
18	1 1 0 1 0 0 0	Device 24
19	1 1 0 1 0 0 1	Device 25
1A	1 1 0 1 0 1 0	Device 26
1B	1 1 0 1 0 1 1	Device 27
1C	1 1 0 1 1 0 0	Device 28
1D	1 1 0 1 1 0 1	Device 29
1E	1 1 0 1 1 1 0	Device 30
1F	1 1 0 1 1 1 1	Device 31
~~	1 0 0 X X X X	No Device (illegal)
ANY	1 X X X X X X	Any Device

Table 2–3 lists the name, bit pattern, and description of the symbols in the file Rambus_ROP, in the Row Opcode channel group symbol table.

Table 2–3: Row Opcode group symbol table definitions

Symbol	Rambus_ROP group value AV ROP10 ROP9 ROW-VALID ROP8 ROP7 ROP6 ROP5 ROP4 ROP3 ROP2 ROP1 ROP0	Description
—	0 X X X X X X X X X X X X	No Row Packet
ACT	1 1 X X X X X X X X X X X	Activate row of bank of device, bring device to Attention
PRER_PDNR_ATTN	1 0 1 1 0 0 0 0 1 0 0 0 0	Precharge bank of device, Power Down device, bring device to Attention
PRER_NAPR_ATTN	1 0 1 1 0 0 0 1 0 0 0 0 0	Precharge bank of device, Nap Down device, bring device to Attention
PRER_NAPRC_ATTN	1 0 1 1 0 0 0 1 1 0 0 0 0	Precharge bank of device, Nap Down device Conditionally, bring device to Attention
PRER_PDNR_RLXR	1 0 1 1 0 0 0 0 1 1 0 0 0	Precharge bank of device, Power Down device, Relax device
PRER_NAPR_RLXR	1 0 1 1 0 0 0 1 0 1 0 0 0	Precharge bank of device, Nap Down device, Relax device
PRER_NAPRC_RLXR	1 0 1 1 0 0 0 1 1 1 0 0 0	Precharge bank of device, Nap Down device Conditionally, Relax device
REFA_ATTN	1 0 0 0 0 1 1 0 0 0 0 0 0	Refresh Row of bank of device, bring device to Attention
REFP_ATTN	1 0 1 0 1 0 1 0 0 0 0 0 0	Precharge bank of device after REFA, bring device to Attention
REFA_RLXR	1 0 0 0 0 1 1 0 0 1 0 0 0	Refresh row of bank of device, Relax device
REFP_RLXR	1 0 1 0 1 0 1 0 0 1 0 0 0	Precharge bank of device after REFA, Relax device
PRER_ATTN	1 0 1 1 0 0 0 X X 0 0 0 0	Precharge bank of device, bring device to Attention
PRER_RLXR	1 0 1 1 0 0 0 X X 1 0 0 0	Precharge bank of device, Relax device
PDNR_ATTN	1 0 X X 0 0 0 0 1 0 0 0 0	Power Down device, bring device to Attention
NAPR_ATTN	1 0 X X 0 0 0 1 0 0 0 0 0	Nap Down device, bring device to Attention
NAPRC_ATTN	1 0 X X 0 0 0 1 1 0 0 0 0	Nap Down device Conditionally, bring device to Attention
PDNR_RLXR	1 0 X X 0 0 0 0 1 1 0 0 0	Power Down device, Relax device
NAPR_RLXR	1 0 X X 0 0 0 1 0 1 0 0 0	Nap Down device, Relax device

Table 2–3: Row Opcode group symbol table definitions (cont.)

Symbol	Rambus_ROP group value ROW-VALID AV ROP10 ROP9 ROP8 ROP7 ROP6 ROP5 ROP4 ROP3 ROP2 ROP1 ROP0	Description
NAPRC_RLXR	1 0 X X 0 0 0 1 1 1 0 0 0	Nap Down device Conditionally, Relax device
PRER_PDNR	1 0 1 1 0 0 0 0 1 X 0 0 0	Precharge bank of device, Power Down device
PRER_NAPR	1 0 1 1 0 0 0 1 0 X 0 0 0	Precharge bank of device, Nap Down device
PRER_NAPRC	1 0 1 1 0 0 0 1 1 X 0 0 0	Precharge bank of device, Nap Down device Conditionally
PRER	1 0 1 1 0 0 0 X X X 0 0 0	Precharge bank of device
REFA	1 0 0 0 0 1 1 0 0 X 0 0 0	Refresh row of bank of device
REFP	1 0 1 0 1 0 1 0 0 X 0 0 0	Precharge bank of device after REFA
PDNR	1 0 X X 0 0 0 0 1 X 0 0 0	Power down device
NAPR	1 0 X X 0 0 0 1 0 X 0 0 0	Nap down device
NAPRC	1 0 X X 0 0 0 1 1 X 0 0 0	Nap down device conditionally
ATTN	1 0 X X X X X X X 0 0 0 0	Bring device to Attention
RLXR	1 0 X X X X X X X 1 0 0 0	Relax device
TCAL	1 0 0 0 0 0 0 0 0 X 0 0 1	Temperature Calibrate device
TCEN	1 0 0 0 0 0 0 0 0 X 0 1 0	Temperature Calibrate/Enable device
NOROP	1 0 0 0 0 0 0 0 0 0 0 0 0	No ROP Operation
ANY	1 X X X X X X X X X X X X	Any Operation

Table 2–4 lists the name, bit pattern, and description of the symbols in the file Rambus_COP, in the Column Opcode channel group symbol table.

Table 2–4: Column Opcode group symbol table definitions

Symbol	Rambus_COP group value COL-VALID S=1 COP3 COP2 COP1 COP0	Description
——	0 X X X X X	No Column Packet
RDA_RLXC	1 1 1 1 1 1	Same as RD, but Precharge Bank afterward, Relax device
	1 1 1 1 1 0	Reserved, no defined operation

Table 2–4: Column Opcode group symbol table definitions (cont.)

Symbol	Rambus_COP group value COL-VALID S=1 COP3 COP2 COP1 COP0	Description
WRA_RLXC	1 1 1 1 0 1	Same as WR, but Precharge Bank of device after Write Buffer is Retired, Relax device
PREC_RLXC	1 1 1 1 0 0	Retire Write Buffer of device, Pre-charge Bank of device, Relax device
RD_RLXC	1 1 1 X 1 1	Read column of bank of device, Relax device
	1 1 1 0 1 0	Reserved, no defined operation
WR_RLXC	1 1 1 X 0 1	Retire Write Buffer of device, Write column of bank to Write Buffer, Relax device
NOCOP_RLXC	1 1 1 0 0 0	Retire Write Buffer, Relax device
RDA	1 1 X 1 1 1	Same as RD, but Precharge Bank afterward
	1 1 X 1 1 0	Reserved, no defined operation
WRA	1 1 X 1 0 1	Same as WR, but Precharge Bank of device after Write Buffer is Retired
PREC	1 1 X 1 0 0	Retire Write Buffer of device, Pre-charge Bank of device
RD	1 1 X X 1 1	Read column of bank of device
	1 1 X 0 1 0	Reserved, no defined operation
WR	1 1 X X 0 1	Retire Write Buffer of device, Write column of bank to Write Buffer
NOCOP	1 1 X 0 0 0	Retire Write Buffer
RLXC	1 1 1 X X X	Relax device
~~	1 0 X X X X	No operation (illegal)
ANY	1 X X X X X	Any operation

Table 2–5 lists the name, bit pattern, and description of the symbols in the file Rambus_XOP, in the XOP Opcode channel group symbol table.

Table 2–5: XOP Opcode group symbol table definitions

Symbol	Rambus_XOP group value COL-VALID S=1 M=0 XOP4 XOP3 XOP2 XOP1 XOP0	Description
—	0 X X X X X X X	No Column Packet
MSK	1 1 1 X X X X X	Byte Mask
NOXOP	1 1 0 0 0 0 0 0	No XOP Operation
PREX_CAL_SAM_RLXX	1 1 0 1 1 1 1 0	Precharge Bank of device, Calibrate, Sample, Relax
PREX_CAL_SAM	1 1 0 1 1 1 X 0	Precharge Bank of device, Calibrate, Sample
PREX_CAL_RLXX	1 1 0 1 1 X 1 0	Precharge Bank of device, Calibrate, Relax
PREX_CAL	1 1 0 1 1 X X 0	Precharge Bank of device, Calibrate
CAL_SAM_RLXX	1 1 0 X 1 1 1 0	Calibrate, Sample, Relax
CAL_SAM	1 1 0 X 1 1 X 0	Calibrate, Sample
CAL_RLXX	1 1 0 X 1 X 1 0	Calibrate, Relax
CAL	1 1 0 X 1 X X 0	Calibrate
PREX_RLXX	1 1 0 1 X X 1 0	Precharge Bank of device, Relax
PREX	1 1 0 1 X X X 0	Precharge Bank of device
RLXX	1 1 0 X X X 1 0	Relax
RSRV	1 1 0 X X X X 1	Reserved, no defined operation
~~	1 0 X X X X X X	No operation (illegal)
ANY	1 X X X X X X X	Any operation

Table 2–6 lists the name, bit pattern, and description of the symbols in the file Rambus_SIO, in the Serial I/O channel group symbol table.

Table 2–6: Serial I/O group symbol table definitions

Symbol	Rambus_SIO group value SIO-1 SIO-0	Description
—	0 0	No NAP/PDN Exit
1	1 0	NAP/PDN Exit, SIO = 1
0	0 1	NAP/PDN Exit, SIO = 0

Table 2–7 lists the name, bit pattern, and description of the symbols in the file Rambus_ROW, in the Row Packet channel group symbol table.

Table 2–7: Row Packet group symbol table definitions

Symbol	Rambus_ROW group value ROW-VALID ROW-TMG1 ROW-TMG0	Description
—	0 X X	No Row Packet
T0	1 0 0	Timing Offset =0
T1	1 0 1	Timing Offset =1
T2	1 1 0	Timing Offset =2
T3	1 1 1	Timing Offset =3
ANY	1 X X	Any Row Packet

Table 2–8 lists the name, bit pattern, and description of the symbols in the file Rambus_COL, in the Column Packet channel group symbol table.

Table 2–8: Column Packet group symbol table definitions

Symbol	Rambus_COL group value COL-VALID COL-TMG1 COL-TMG0	Description
—	0 X X	No Column Packet
T0	1 0 0	Timing Offset =0
T1	1 0 1	Timing Offset =1
T2	1 1 0	Timing Offset =2

Table 2–8: Column Packet group symbol table definitions (cont.)

Symbol	Rambus_COL group value COL-VALID COL-TMG1 COL-TMG0	Description
T3	1 1 1	Timing Offset =3
ANY	1 X X	Any Column Packet

Timing Alignment Between Packets

While acquiring the Row, Column, and Write Data packets, a timing error is introduced between packets.

In the display window, whenever a Row packet is acquired, T0, T1, T2 or T3 is displayed in the ROW column indicating the presence of a Row packet. Whenever a Column packet is acquired, the COL column will indicate T0, T1, T2, or T3 indicating the presence of a Column packet. A dash in the ROW column indicates a particular row packet was not present. A dash in the COL column indicates a particular column packet was not present (see Figure 2–4 on page 2–18).

To determine the actual time between any two packets, you must first determine the amount of time between the corresponding two samples. One method of determining this time difference is to use the Delta (Δ) time measurement feature on the logic analyzer. A second way, is to determine the difference between the timestamps of the two samples. In either case, add or subtract from 0 to 3 Rambus clock cycles. The following Table 2–9 is used to determine the time between any two Row packets, any two Column packets, or between any two Row and Column packets.

Table 2–9: Rambus Clock Cycle Time Differences

Earlier sample	Later sample			
	T0	**T1**	**T2**	**T3**
T0	0	+1	+2	+3
T1	–1	0	+1	+2
T2	–2	–1	0	+1
T3	–3	–2	–1	0

Even if two packets are acquired on the same sample; the packet with the smaller number occurred earlier than the packet with the larger number, and the

difference between the two numbers indicate the difference in Rambus clock cycles.

Because Write Data packets always follow their associated Column packets by 10 Rambus clock cycles, they are acquired on the same sample as the Column packet. This was done to aid triggering on a combination of Column packets and Write Data packets. As a result, when trying to determine the time between Write Data packets and any other Row or Column packets, you must account for the fact that the Write Data packet actually occurred 10 Rambus clock cycles later than indicated by its associated Column packet. This can cause confusion relative to Mask Bytes (COLM packets). These 10 clock cycles are measured from the end of the Column packet to the end of the Write Data packet.

SIO Timing

The SIO bus Power State Transitions of NAP/PDN Exit are also shown 10 Rambus clock cycles earlier than they actually occurred on the SIO bus. This is because the SIO bus runs from its own SCK clock, and that clock, while running at one fourth the clock rate of the Rambus, has no specified phase relationship to the Rambus CFM clock.

As a result, depending upon the phase relationship between those two clocks, it is possible for a single Power State Transition of NAP/PDN Exit to appear as two consecutive samples. When this happens, those two consecutive samples will have a difference in their timestamps of four Rambus clock cycles (that is 10 ns for a 400 MHz Rambus clock).

If this is occurring on your system, you can adjust the SIO group Setup/Hold Window using the following steps:

1. Select the Setup window, and click on the More button.
2. Scroll down to the SIO group, and then click on the Support Package Default, which is the same as the 1 ns/ 1 ns of Setup and Hold.
3. Adjust the Setup/Hold Window in 500 ps increments until these errors go away, starting with 1.5 ns/500 ps through 2 ns/0 ns.

If this adjustment does not eliminate these errors, you may try going in the opposite direction, starting with 500 ps/1.5 ns through 0 ns/2 ns. If you go beyond this range of adjustment these errors will not be visible. After completing this adjustment save this setup for future use.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled.

Acquiring Data

Once you load the Rambus support and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

NOTE*. If either of the following conditions occur you must reset the probe adapter or you will acquire incorrect data: any time the clock has been stopped and restarted or power to the SUT is turned off and on again (see Figure 1–6 on page 1–10 for the Reset switch location). Pressing the Reset button has no effect on the SUT.*

Viewing Disassembled Data

You can view disassembled data in one mode: Show All.

The default display format shows the ROP, DRA, BRA, RA, ROW, COP, DCA, BCA, CA, XOP, DXA, BXA, MA, MB, COL, D0[63:32], D0[31:00], and SIO channel group values for each sample of acquired data. Channel groups D1[63:32] and D1[31:00] are displayed on the second line, below D0[63:32] and D0[31:00].

The D0[63:32], D0[31:00], D1[63:32], and D1[31:00] groups display the data in Front Side Bus byte order. If you want to see the data displayed in Rambus Transmission order, turn off the D0[63:32] and D0[31:00] groups, and turn on the DA[63:32] and DA[31:00] groups. DB[63:32] and DB[31:00] will be displayed on the second line, below DA[63:32] and DA[31:00].

If a channel group is not visible, you must use the Column property page to make the group visible.

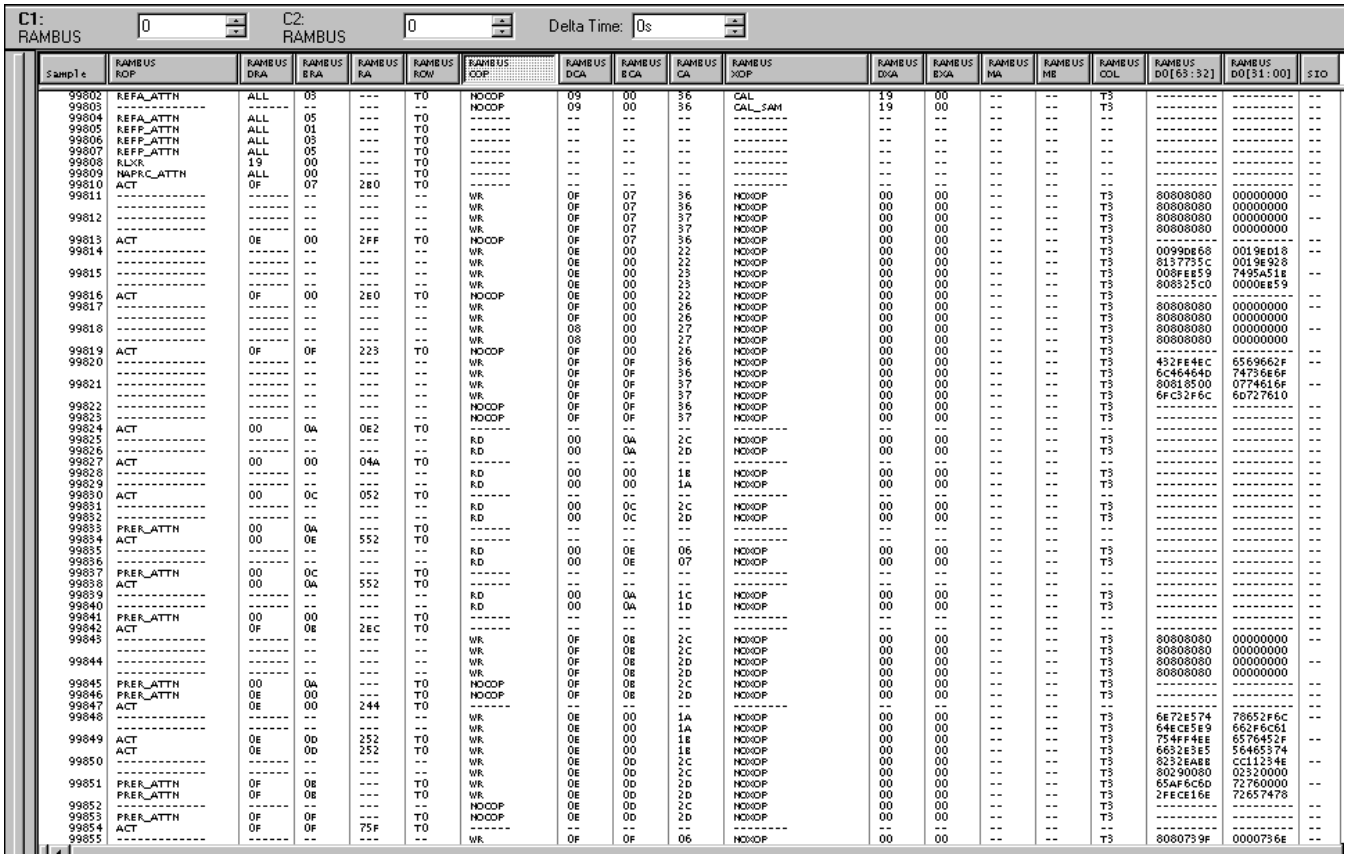
The disassembler displays special characters and strings to indicate significant events. Table 2–10 shows these special characters and strings, and gives a definition of what they represent.

Table 2–10: Description of special characters in the display

Character or string displayed	Definition
>>	There is insufficient room on the screen to show all available data.
––	This indicates invalid data or group, including read data.

Default Listing-Window Format

Figure 2–4 shows an example of a disassembled Listing-Window display format.



Sample	RAMBUS ROP	RAMBUS DRA	RAMBUS BRA	RAMBUS RA	RAMBUS ROW	RAMBUS COP	RAMBUS DCA	RAMBUS BCA	RAMBUS CA	RAMBUS XOP	RAMBUS DXA	RAMBUS BXA	RAMBUS MA	RAMBUS ME	RAMBUS COL	RAMBUS D0[63:32]	RAMBUS D0[31:00]	SIO
99802	REFA_ATTN	ALL	03	---	T0	NOCOP	09	00	36	CAL	19	00	--	--	T3	---------	---------	--
99803	----------	------	--	---	--	NOCOP	09	00	36	CAL_SAM	19	00	--	--	T3	---------	---------	--
99804	REFA_ATTN	ALL	05	---	T0	------	--	--	--	--------	--	--	--	--	--	---------	---------	--
99805	REFP_ATTN	ALL	01	---	T0	------	--	--	--	--------	--	--	--	--	--	---------	---------	--
99806	REFP_ATTN	ALL	03	---	T0	------	--	--	--	--------	--	--	--	--	--	---------	---------	--
99807	REFP_ATTN	ALL	05	---	T0	------	--	--	--	--------	--	--	--	--	--	---------	---------	--
99808	RLXR	19	00	---	T0	------	--	--	--	--------	--	--	--	--	--	---------	---------	--
99809	NAPRC_ATTN	ALL	00	---	T0	------	--	--	--	--------	--	--	--	--	--	---------	---------	--
99810	ACT	0F	07	280	T0	------	--	--	--	--------	--	--	--	--	--	---------	---------	--
99811	----------	------	--	---	--	WR	0F	07	36	NOXOP	00	00	--	--	T3	80808080	00000000	--
	----------	------	--	---	--	WR	0F	07	36	NOXOP	00	00	--	--	T3	80808080	00000000	
99812	----------	------	--	---	--	WR	0F	07	37	NOXOP	00	00	--	--	T3	80808080	00000000	--
	----------	------	--	---	--	WR	0F	07	37	NOXOP	00	00	--	--	T3	80808080	00000000	
99813	ACT	0E	00	2FF	T0	NOXOP	0F	07	36	NOXOP	00	00	--	--	T3	---------	---------	--
99814	----------	------	--	---	--	WR	0E	00	22	NOXOP	00	00	--	--	T3	0099DE68	0019ED18	--
	----------	------	--	---	--	WR	0E	00	22	NOXOP	00	00	--	--	T3	8137755C	0019E928	
99815	----------	------	--	---	--	WR	0E	00	23	NOXOP	00	00	--	--	T3	008FEE59	7495A518	--
	----------	------	--	---	--	WR	0E	00	23	NOXOP	00	00	--	--	T3	808325C0	0000E859	
99816	ACT	0F	00	2E0	T0	NOXOP	0E	00	22	NOXOP	00	00	--	--	T3	---------	---------	--
99817	----------	------	--	---	--	WR	0F	00	26	NOXOP	00	00	--	--	T3	80808080	00000000	--
	----------	------	--	---	--	WR	0F	00	26	NOXOP	00	00	--	--	T3	80808080	00000000	
99818	----------	------	--	---	--	WR	08	00	27	NOXOP	00	00	--	--	T3	80808080	00000000	--
	----------	------	--	---	--	WR	08	00	27	NOXOP	00	00	--	--	T3	80808080	00000000	
99819	ACT	0F	0F	223	T0	NOXOP	0F	0F	26	NOXOP	00	00	--	--	T3	---------	---------	--
99820	----------	------	--	---	--	WR	0F	0F	36	NOXOP	00	00	--	--	T3	432FE4EC	6569662F	--
	----------	------	--	---	--	WR	0F	0F	36	NOXOP	00	00	--	--	T3	6c46464D	74736E6F	
99821	----------	------	--	---	--	WR	0F	0F	37	NOXOP	00	00	--	--	T3	80818500	0774616F	--
	----------	------	--	---	--	WR	0F	0F	37	NOXOP	00	00	--	--	T3	6FC52F6C	6D727610	
99822	----------	------	--	---	--	NOCOP	0F	0F	36	NOXOP	00	00	--	--	T3	---------	---------	--
99823	----------	------	--	---	--	NOCOP	0F	0F	37	NOXOP	00	00	--	--	T3			--
99824	ACT	00	0A	0E2	T0	------	--	--	--	--------	--	--	--	--	--	---------	---------	--
99825	----------	------	--	---	--	RD	00	0A	2C	NOXOP	00	00	--	--	T3	---------	---------	--
99826	----------	------	--	---	--	RD	00	0A	2D	NOXOP	00	00	--	--	T3	---------	---------	--
99827	ACT	00	00	04A	T0	------	--	--	--	--------	--	--	--	--	--	---------	---------	--
99828	----------	------	--	---	--	RD	00	00	1E	NOXOP	00	00	--	--	T3	---------	---------	--
99829	----------	------	--	---	--	RD	00	00	1A	NOXOP	00	00	--	--	T3	---------	---------	--
99830	ACT	00	0C	052	T0	------	--	--	--	--------	--	--	--	--	--	---------	---------	--
99831	----------	------	--	---	--	RD	00	0C	2C	NOXOP	00	00	--	--	T3	---------	---------	--
99832	----------	------	--	---	--	RD	00	0C	2D	NOXOP	00	00	--	--	T3	---------	---------	--
99833	PRER_ATTN	00	0A	---	T0	------	--	--	--	--------	--	--	--	--	--	---------	---------	--
99834	ACT	00	0E	552	T0	------	--	--	--	--------	--	--	--	--	--	---------	---------	--
99835	----------	------	--	---	--	RD	00	0E	06	NOXOP	00	00	--	--	T3	---------	---------	--
99836	----------	------	--	---	--	RD	00	0E	07	NOXOP	00	00	--	--	T3	---------	---------	--
99837	PRER_ATTN	00	0C	---	T0	------	--	--	--	--------	--	--	--	--	--	---------	---------	--
99838	ACT	00	0A	552	T0	------	--	--	--	--------	--	--	--	--	--	---------	---------	--
99839	----------	------	--	---	--	RD	00	0A	1C	NOXOP	00	00	--	--	T3	---------	---------	--
99840	----------	------	--	---	--	RD	00	0A	1D	NOXOP	00	00	--	--	T3	---------	---------	--
99841	PRER_ATTN	00	00	---	T0	------	--	--	--	--------	--	--	--	--	--	---------	---------	--
99842	ACT	0F	08	2EC	T0	------	--	--	--	--------	--	--	--	--	--	---------	---------	--
99843	----------	------	--	---	--	WR	0F	08	2C	NOXOP	00	00	--	--	T3	80808080	00000000	--
	----------	------	--	---	--	WR	0F	08	2C	NOXOP	00	00	--	--	T3	80808080	00000000	
99844	----------	------	--	---	--	WR	0F	08	2D	NOXOP	00	00	--	--	T3	80808080	00000000	--
	----------	------	--	---	--	WR	0F	08	2D	NOXOP	00	00	--	--	T3	80808080	00000000	
99845	PRER_ATTN	00	0A	---	T0	NOCOP	0F	08	2C	NOXOP	00	00	--	--	T3	---------	---------	--
99846	PRER_ATTN	0E	00	---	T0	NOCOP	0F	08	2D	NOXOP	00	00	--	--	T3	---------	---------	--
99847	ACT	0E	00	244	T0	------	--	--	--	--------	--	--	--	--	--	---------	---------	--
99848	----------	------	--	---	--	WR	0E	00	1A	NOXOP	00	00	--	--	T3	6E72E574	78652F6C	--
	----------	------	--	---	--	WR	0E	00	1A	NOXOP	00	00	--	--	T3	64ECE5E9	662F6C61	
99849	ACT	0E	0D	252	T0	WR	0E	00	1E	NOXOP	00	00	--	--	T3	754FF4EE	6576452F	--
	ACT	0E	0D	252	T0	WR	0E	00	1E	NOXOP	00	00	--	--	T3	6632E3E5	56465374	
99850	----------	------	--	---	--	WR	0E	0D	2C	NOXOP	00	00	--	--	T3	8232EABB	CC11234E	--
	----------	------	--	---	--	WR	0E	0D	2C	NOXOP	00	00	--	--	T3	80290080	02320000	
99851	PRER_ATTN	0F	08	---	T0	WR	0E	0D	2D	NOXOP	00	00	--	--	T3	65AF6C6D	72760000	--
	PRER_ATTN	0F	08	---	T0	WR	0E	0D	2D	NOXOP	00	00	--	--	T3	2FECE16E	72657478	
99852	----------	------	--	---	--	NOCOP	0E	0D	2C	NOXOP	00	00	--	--	T3	---------	---------	--
99853	PRER_ATTN	0F	0F	---	T0	NOCOP	0E	0D	2D	NOXOP	00	00	--	--	T3	---------	---------	--
99854	ACT	0F	0F	75F	T0	------	--	--	--	--------	--	--	--	--	--	---------	---------	--
99855	----------	------	--	---	--	WR	0F	0F	06	NOXOP	00	00	--	--	T3	8080739F	0000736E	--

Figure 2–4: Disassembled display format

Invalid groups. The disassembler will invalidate any group that is not valid for a given sample. The disassembler uses dashes to represent invalid groups.

For example; if a sample is acquired and a Row packet is not present, all groups associated with a Row packet, DRA, BRA, RA, and ROP groups, are represented as a dash. Also, if a sample is acquired and a Column packet is not present, all groups associated with a Column packet are represented as a dash.

Searching Through Data. Data searching is supported in the listing display.

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your Rambus Direct bus cycles look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your system under test.

To view the TMS 810 Rambus Direct demonstration file, follow these steps:

1. From the Window menu, select Load Data Window. Click Browse.
2. Move down through the directory structure as follows:
   `C:\Program files\TLA700\Supports\RAMBUS\Demo.tla`
3. Click Open. Click Open again.

The Listing window shows an example of disassembled data.

Setup and Display for Cross-Trigger

The purpose of this procedure is to allow you to interface the TDS694C Oscilloscope with the Tektronix Logic Analyzer (TLA) using a TMS 810 probe adapter. Interfacing the TDS694C Oscilloscope with the logic analyzer will increase your capacity to analyze and troubleshoot Rambus signals.

The TDS694C Oscilloscope has a 3 GHz analog bandwidth feeding a 10 GS/s sample rate. This sample rate combined with a memory depth of 120,000 samples allows for 12 μS capture depth (effective memory depth). Note that there is no performance penalty for using all 4 probe channels on your TDS694C at one time.

The TMS 810 probe adapter is a custom interface used to deserialize Rambus from 800 MS/s data rate to 100 MS/s parallel data rate.

If you are not familiar with Rambus protocol, it would be to your benefit to visit the Rambus web sight at www.rambus.com to familiarize yourself with Rambus protocol. In this procedure, Rambus protocols are encoded into packets defined as serial data. The word serial, in this case, is used to mean 3, 5, or 8 bits wide. The Rambus specification will define the entire group as protocol. For example, 3 bits wide times an 8 bit long packet.

The term serial bus is used loosely to describe how protocol is encoded. As background to understanding the system architecture, data may travel in a wide parallel Front Side Bus (FSB) from the processor to the memory controller and leaves this chip set at a compressed 800 MS/s data rate. Every 8 bits of 100 MS/s

on the FSB has been compressed into 1 bit of 800 MS/s data, but in packets that are 8 bits long.

The relationship between ROW, COLUMN, and DATA is critical and needs to be tracked from reset particularly during high percentage use of the Rambus channel. The beginning of a row packet has no absolute encoded start of packet indication and the Column packet also has no absolute encoded start of packet indication. In contrast, DATA packets do have a fixed relationship to Column packets. DATA packets follow Column packets by 10 CFM clock cycles, although not all Column packets are followed by data packets.

The TMS 810 support tracks from reset or beginning of activity and establishes an arbitrary starting point as zero. The difference from zero is reported as T#s or clock cycles from this arbitrary sample starting point. While there is a separate T# for Row and a separate T# for Column, both reference the same arbitrary starting clock cycle. These two T#s may change dynamically from packet to packet. Remember that a packet is 8 samples long or 4 complete CFM Rambus clock cycles. So the T#s are going to be T0, T1, T2, or T3.

The TMS 810 is the probe adapter that plugs into a Rambus Direct RIMM Module replacing one memory module and interfaces with the logic analyzer. Please refer to the *Operating Basics* chapter beginning on page 2-1 for a detailed operational description.

Connecting the Oscilloscope to the Logic Analyzer

To hook a TDS694C Tektronix Oscilloscope to the logic analyzer, a P6041 adapter cable needs to be connected between the logic analyzer System Trigger Out and the Auxiliary Trigger Input at the rear of the TDS694C Oscilloscope. The oscilloscope probes can now be connected to the Rambus signals of interest. It may be the easiest to probe these signals on the under side of the motherboard. In the event that this will not work, refer to the schematics located in chapter five. The next step is to properly configure the TDS694C Oscilloscope as follows:

Setting the TDS Delay

1. Press the **Trigger** menu button, and then choose **Source**> **more**> **Tla Cross Trigger delay**.

2. Using the keypad, enter the TDS delay from the following table:

System Set Clock	TDS Delay
400 MHz	502 ns
356 MHz	521 ns
300 MHz	557 ns

3. Choose **Tla Cross Trigger delay** again after entering the TDS delay. This turns off the TLA cross trigger selection and prevents accidentally moving the value with the scroll knob.

Trigger and Horizontal Menu Steps

4. Press the **Trigger Menu** button, and then choose **Slope**> **falling**.
5. Press the **Trigger Menu** button, and then choose **Level**> **Set to TTL**.
6. Press the **Trigger Menu** button, and then choose **Mode & Holdoff**> **Normal**.
7. Press the **Horizontal Menu** button, and then choose **Record Length**> **more**> **more**>**120,000 points in 2400 divs**.
8. Determine which channel to set up for Rambus signal levels, and then press the corresponding **Channel** button (CH1, CH2, CH3, or CH4).

Vertical Menu Steps

9. Press the **Vertical Menu** button, and then choose **Fine Scale**. Using the keypad, enter 200 m.
10. Press the **Vertical Menu** button, and then choose **Position**. Using the keypad, enter 0.
11. Press the **Vertical Menu** button, and then choose **Offset**. Using the keypad, enter 1.2.

Repeat steps 9 through 11 for each channel to set up for Rambus signal levels.

Running the Application

12. Set the horizontal scale to 5 ns/div. Note that the sample rate will be 10 GS/s.
13. Press the **Zoom** button and choose **On**.
14. Press the **Run/Stop** button.

Trigger Setting. Please refer to the *Tektronix Logic Analyzer Family User Manual* for the logic analyzer setup. It is important to set the trigger for "Trigger All Modules". A regular trigger definition in the trigger menu will not assert a trigger on the trigger out of the logic analyzer SMB connector used to feed the oscilloscope.

Rambus Protocol. Rambus is a protocol intensive bus. Understanding this protocol will enable you to perform advanced diagnostics on the bus.

Since the bus is 26 bits wide, the 3 serial buses will add up to 26 bits in width. Three bits are Row, five bits are Column, eight bits are DQA0..7, eight bits are DQB0..7, one bit is parity for DQA and one bit is parity for DQB. This adds up to 26 (3+5+8+8+1+1=26).

Note that Row and Column have multiple functions and are described in the Rambus specification on www.rambus.com. In the TMS810 support, the beginning of all these packets are tracked from reset and displayed in a parallel form. Please refer to the *Operating Basics* chapter beginning on page 2-1 for detailed information on how this protocol has been partitioned and the capability available.

The Rambus specification makes it clear that only the parallel or deserialized representation of Rambus can represent a decoded look at the bus. Additionally, it is critical that the beginning of these packets are known. The Tektronix support has performed a clean reconstruction of the protocol in parallel form with the T#s to allow you to determine the precise relationship. Review of the T#s will give you the packet in question and allow for reading the display to gain the precise edge of interest.

Data Bits Displayed on the TDS694C Oscilloscope. The logic analyzer will now trigger the TDS oscilloscope on a trigger event defined in the logic analyzer trigger menu. Please test this out to ensure that a trigger is successfully achieved. Rambus activity occurs in bursts and is separated by times that vary. Figure 2–5 shows that during high bus activity, there are multiple bursts of activity and you can see that the separation between bursts compares to the logic analyzer separation.

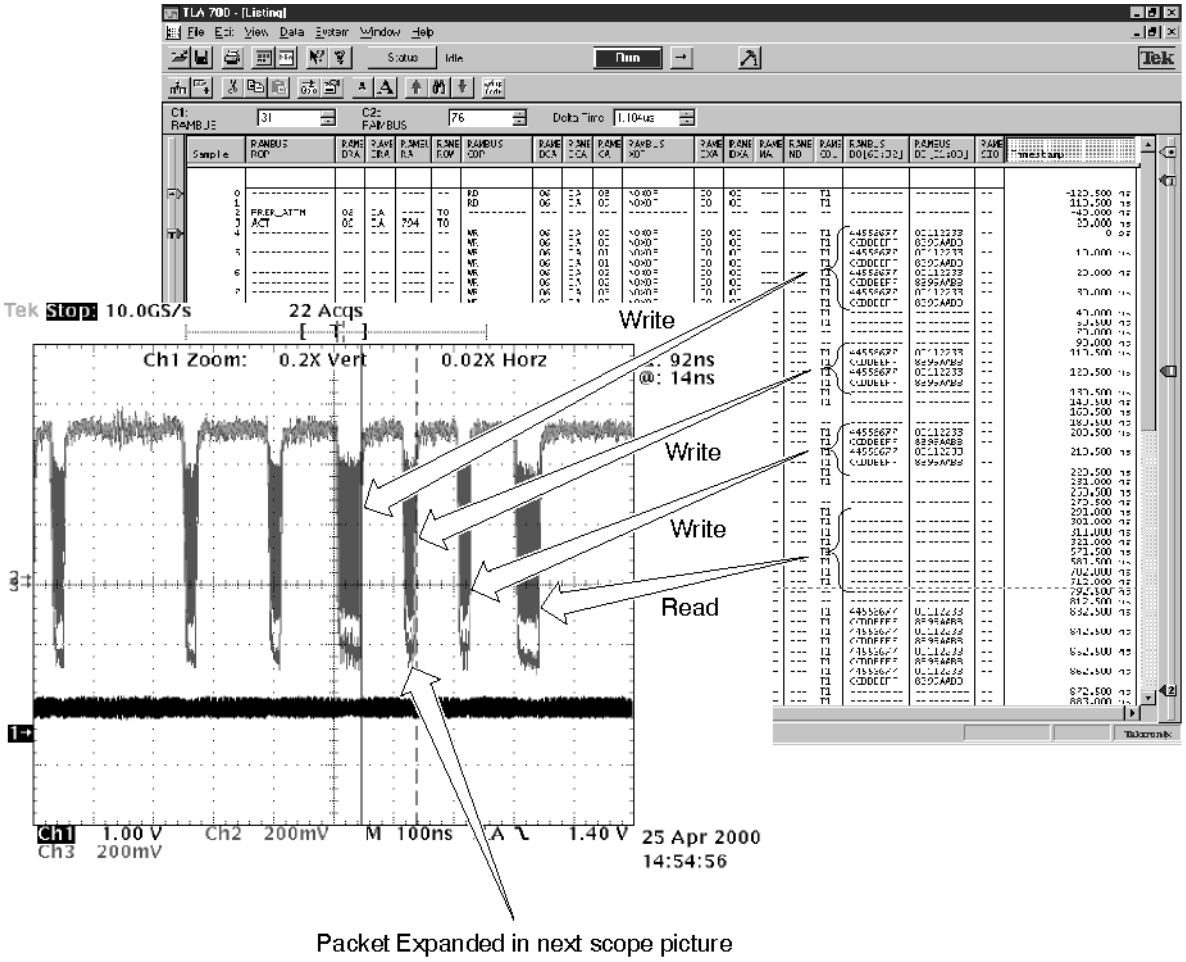


Figure 2–5: Data bits displayed on the oscilloscope

Examples. Figures 2–6 through 2–13 show one full packet for DQA0 and DQA1. They show how the logic analyzer bytes are related to the TDS oscilloscope display. Please refer to the chapter on operating basics for clarification and explanation of various orders such as FSB order, Rambus order, and the affect of having ECC on the bios. This example has ECC=OFF in the bios and uses the stacked method with D0 and then D1. Note that the bytes making up one packet are stacked on two lines. Tektronix calls the first line D0 and the second line D1. This stacking method saves screen width; however, the actual bit numbers in the logic analyzer display may appear misleading due to this method of display.

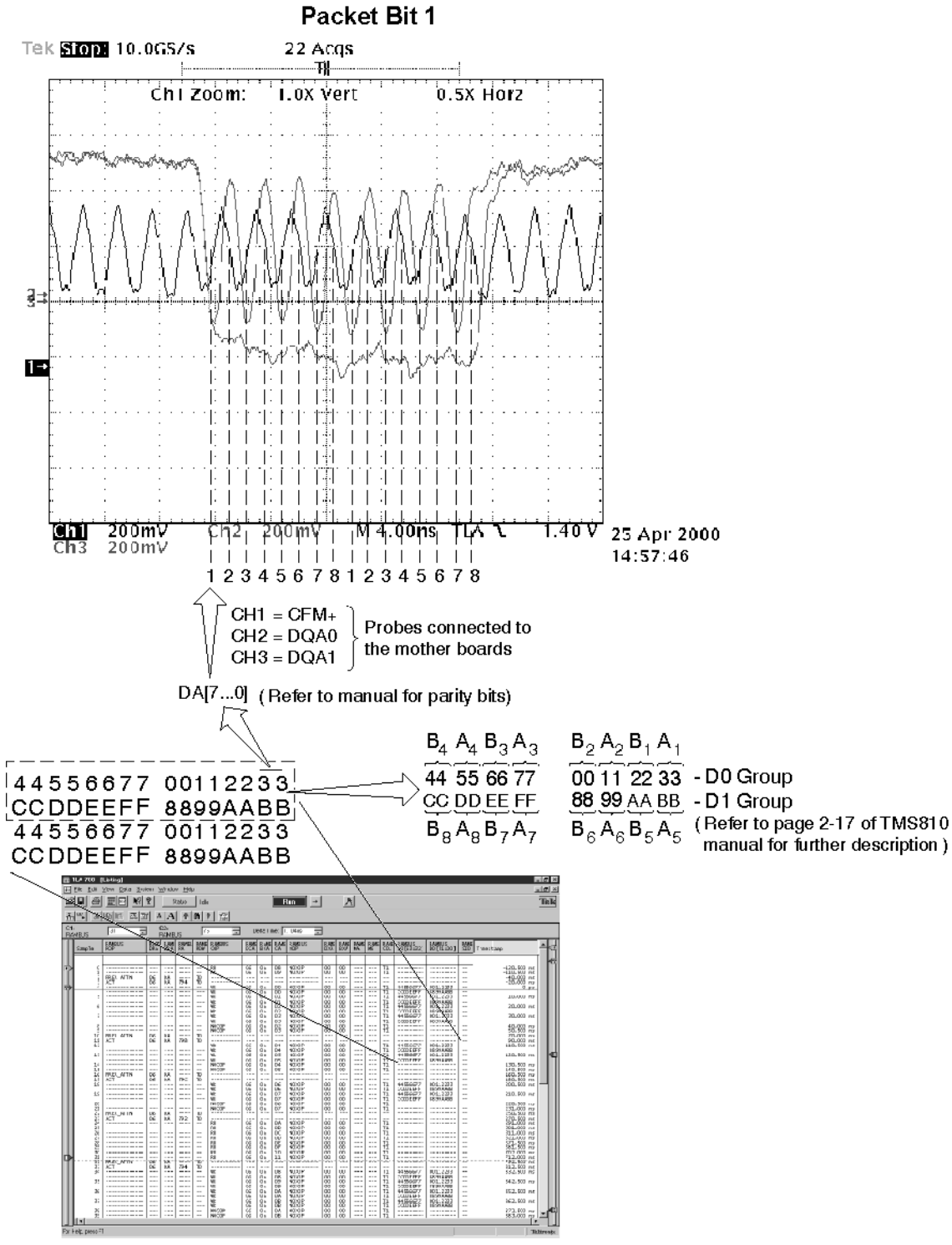


Figure 2–6: Expanded View of Packet Bit 1

Note that 33 corresponds to the bit 1 packet.

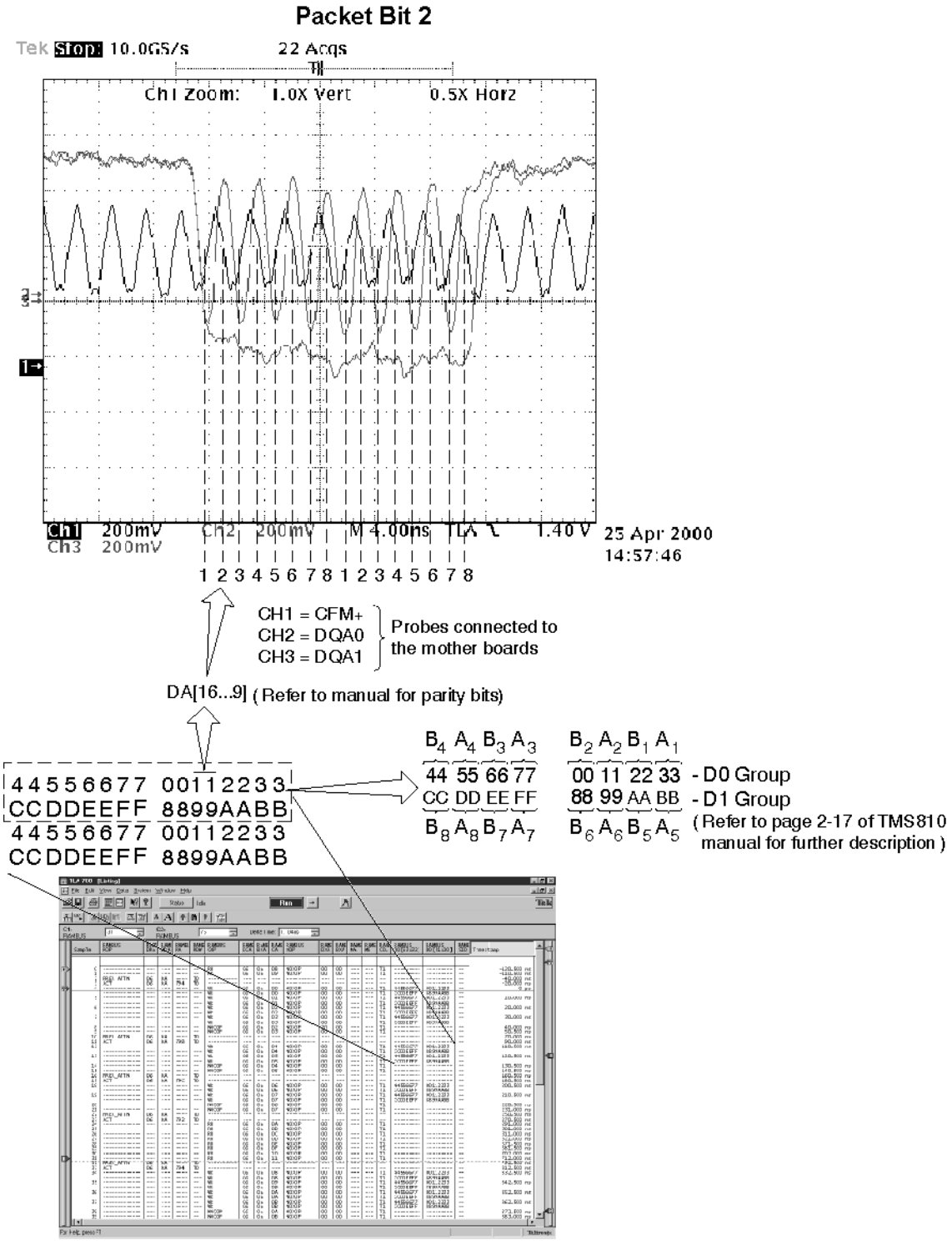


Figure 2–7: Expanded View of Packet Bit 2

Note that 22 is skipped and that 11 corresponds to the bit 2 packet.

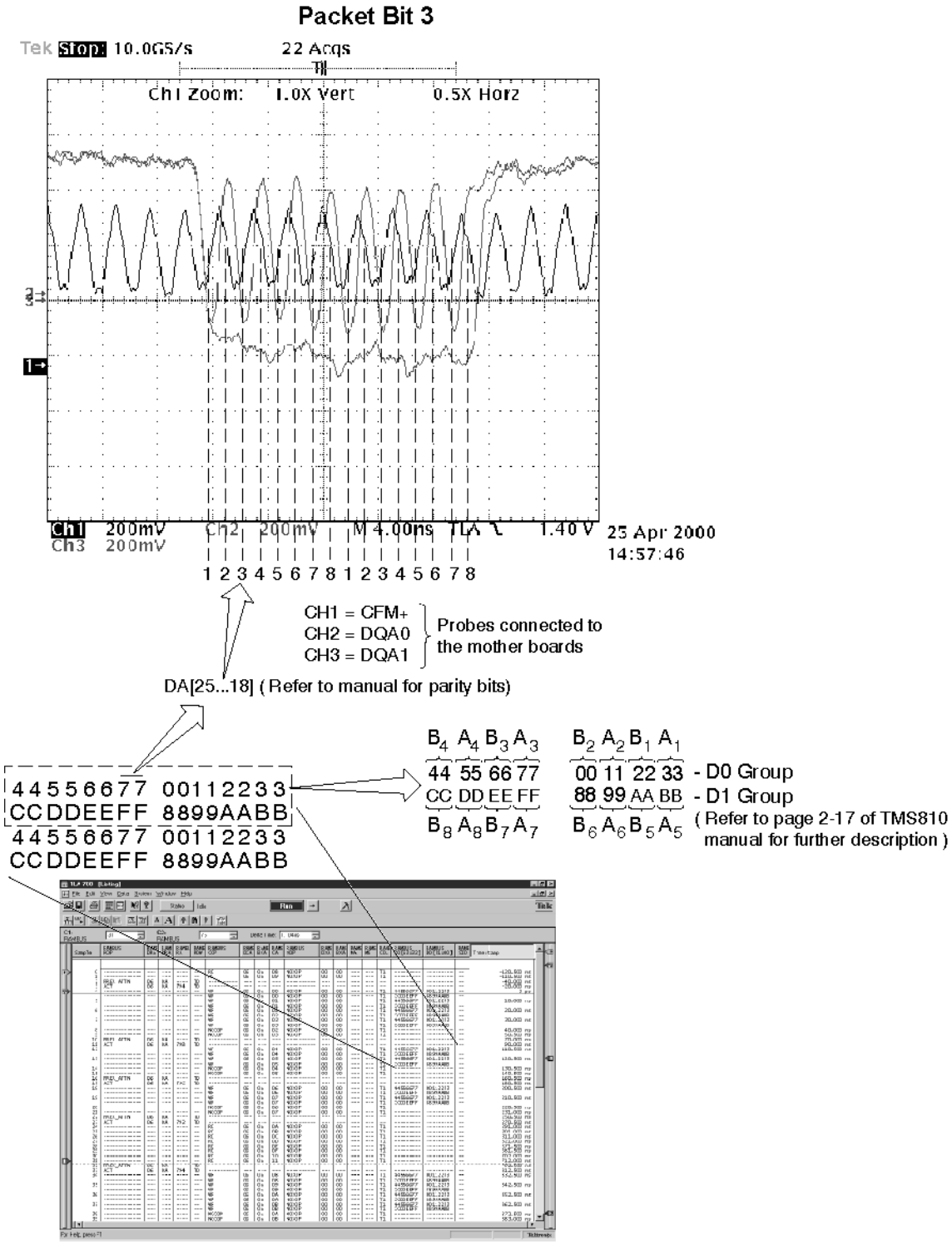


Figure 2–8: Expanded View of Packet Bit 3

Note that 00 is skipped and that 77 corresponds to the bit 3 packet.

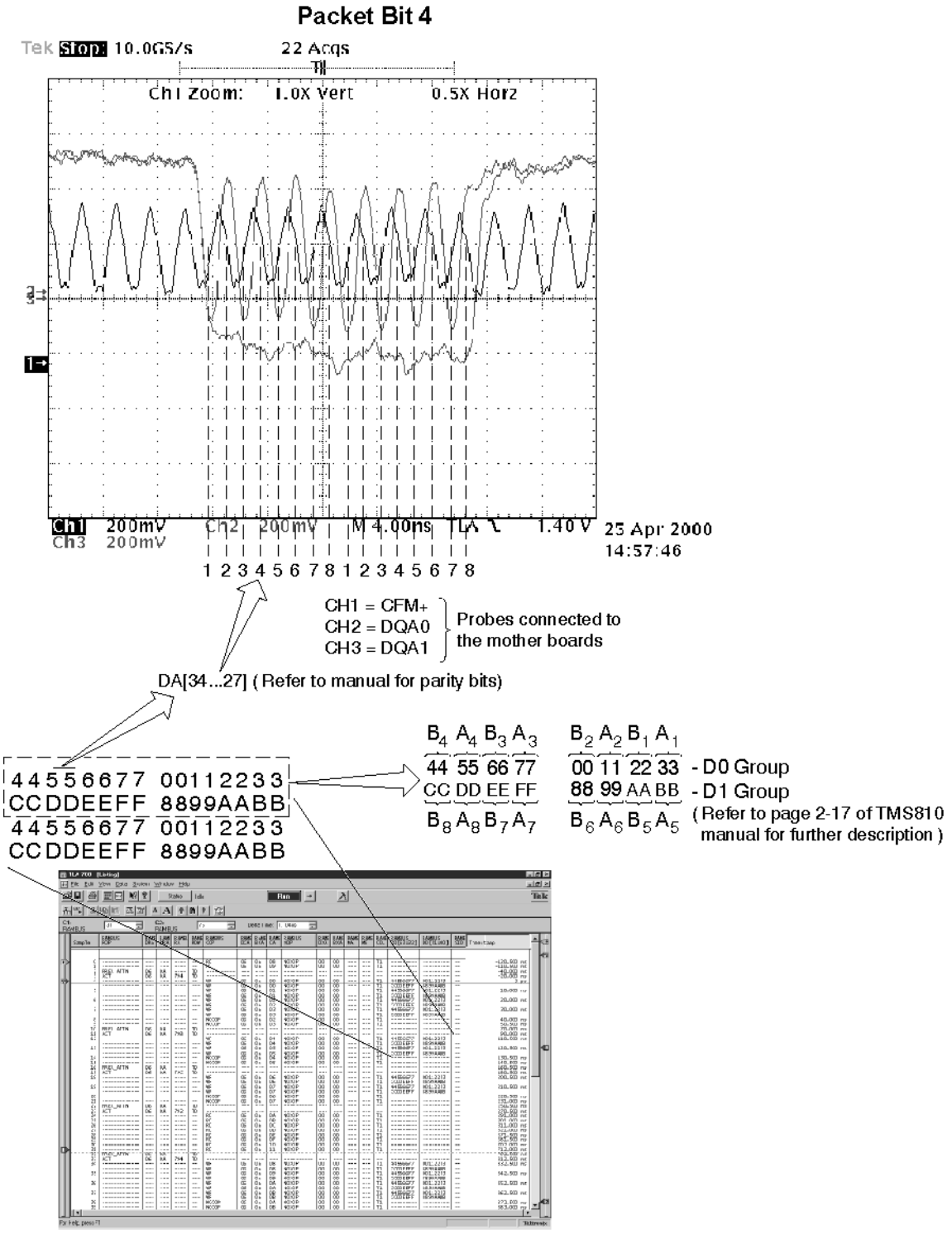


Figure 2–9: Expanded View of Packet Bit 4

Note that 66 is skipped and that 55 corresponds to the bit 4 packet.

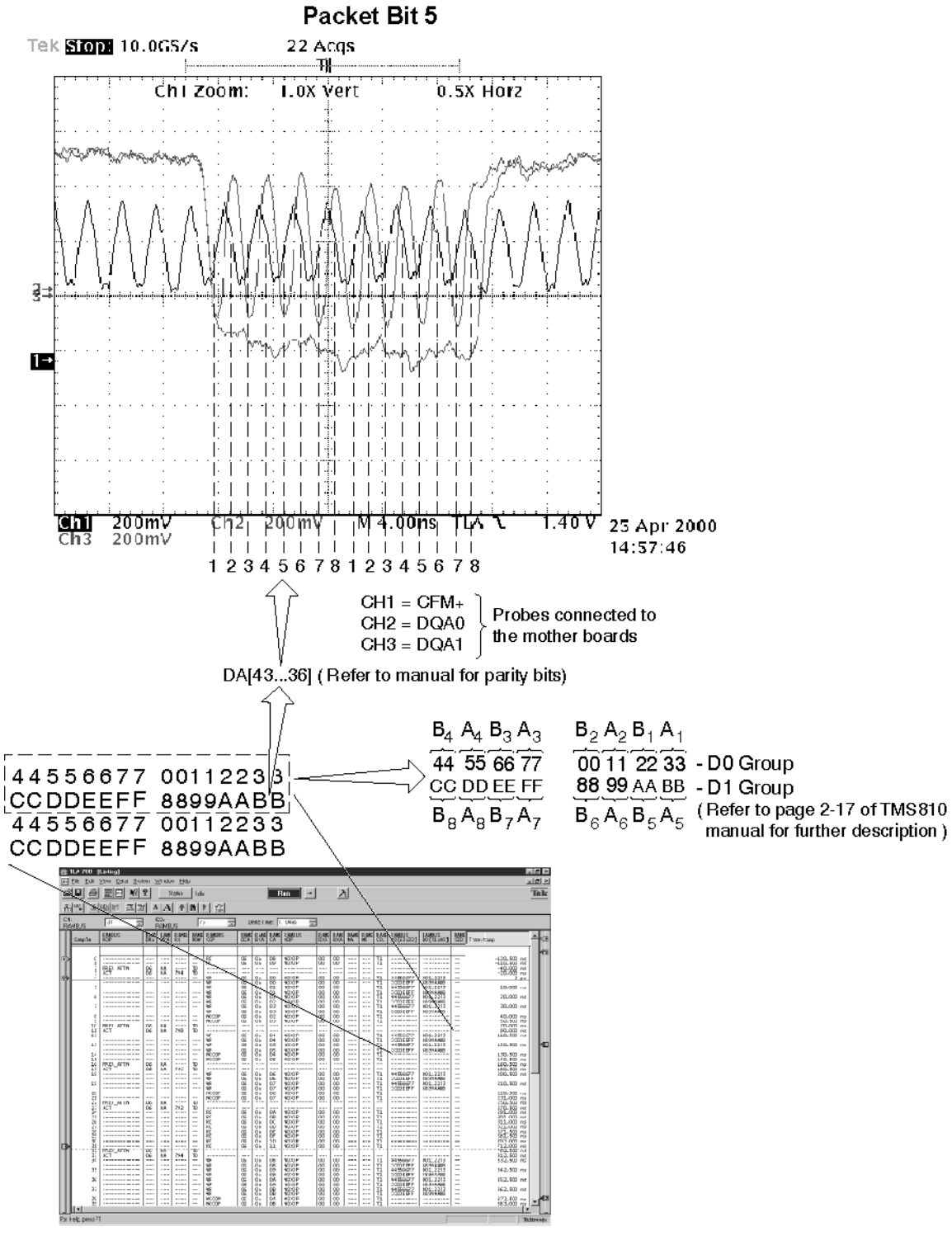


Figure 2–10: Expanded View of Packet Bit 5

Note that 44 is skipped and that BB corresponds to the bit 5 packet.

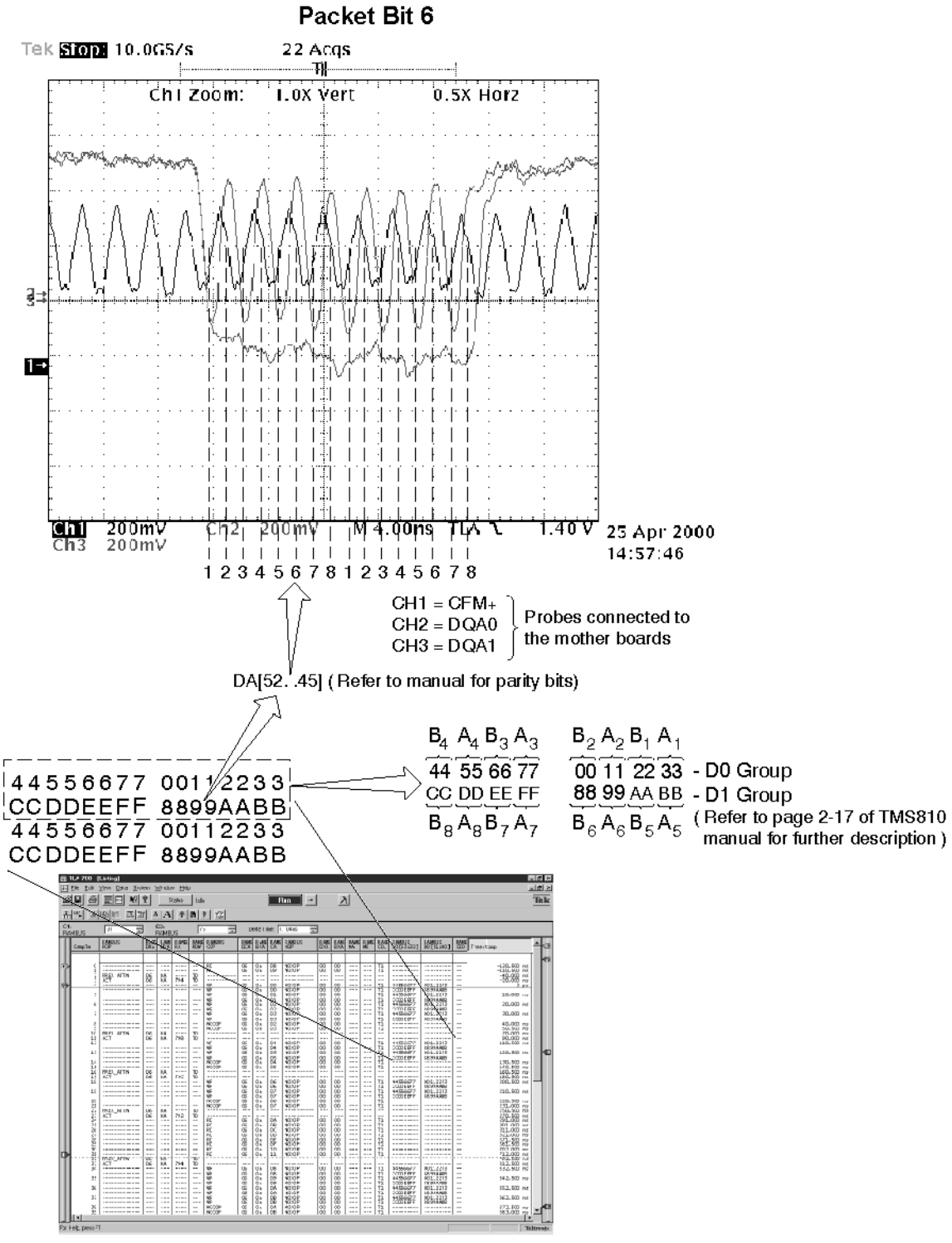


Figure 2–11: Expanded View of Packet Bit 6

Note that AA is skipped and that 99 corresponds to the bit 6 packet.

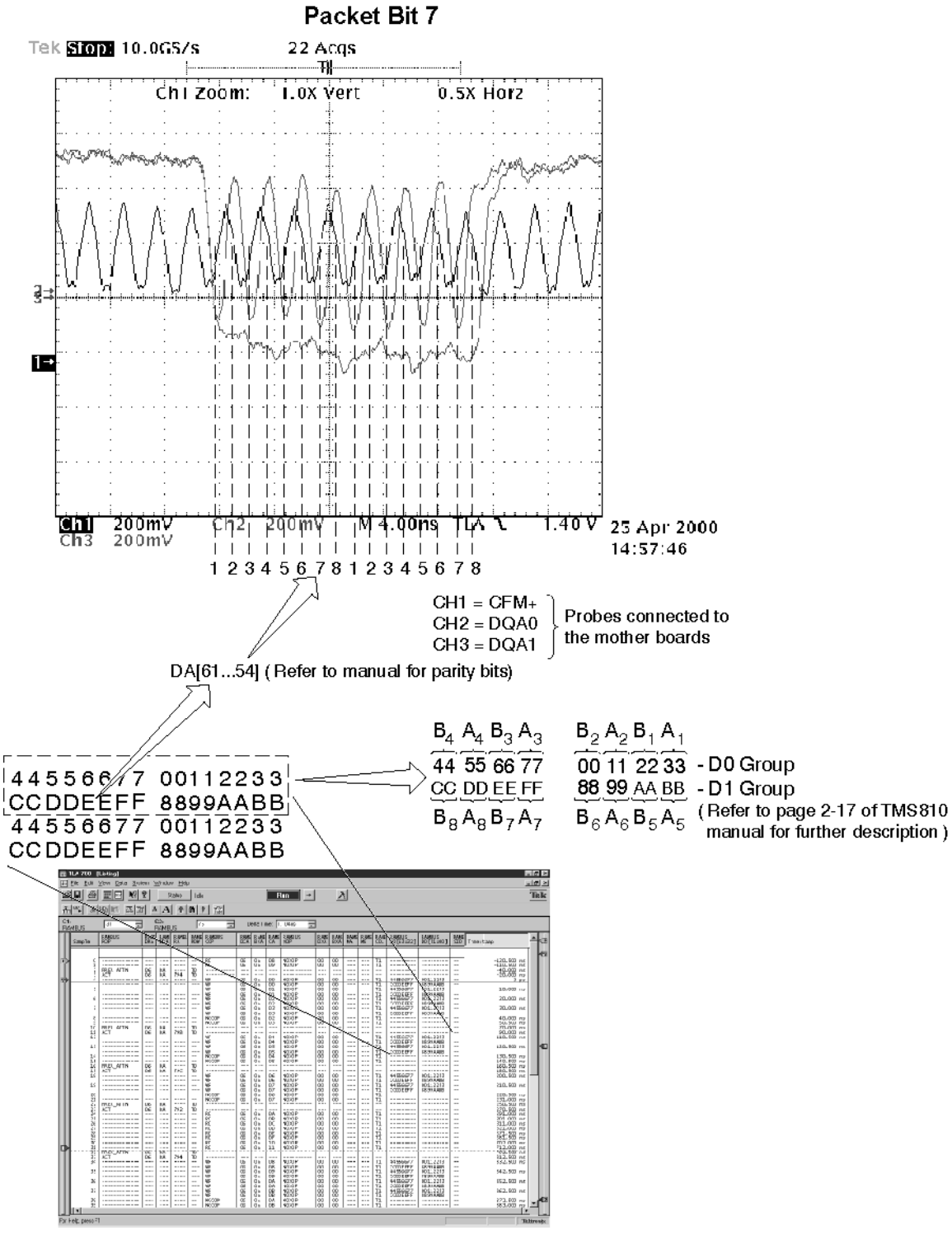


Figure 2–12: Expanded View of Packet Bit 7

Note that 88 is skipped and that EE corresponds to the bit 7 packet.

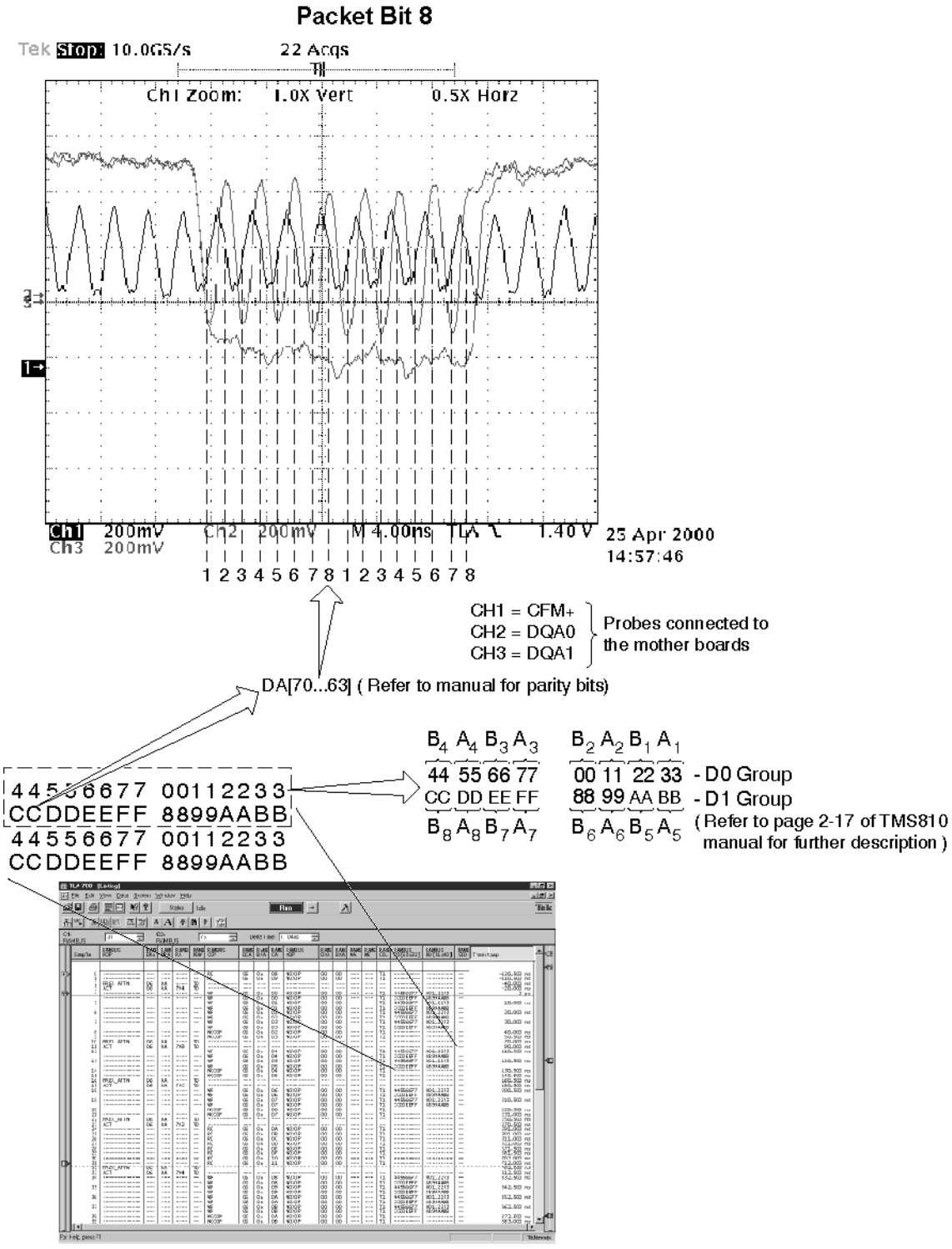


Figure 2–13: Expanded View of Packet Bit 8

Note that DD is skipped and that CC corresponds to the bit 8 packet.

Specifications

Specifications

This chapter contains information regarding the specifications of the TMS 810 Rambus Direct support.

Specification Tables

Table 3–1 lists the electrical requirements the system under test must produce for the support to acquire correct data.

Table 3–1: Electrical specifications

Characteristics	Requirements	
Probe Adapter AC power requirements		
Voltage	90 – 265 VAC	
Current	1.1 A at 100 VAC	
Frequency	47 – 63 Hz	
Power output (each power supply)	5 V, 25 W Maximum	
SUT clock rate		
Specified clock rate	Maximum 400 MHz	
SCK clock rate[1]	Maximum 100 MHz	
Minimum setup time required	0.2 ns	
Minimum hold time required	0.2 ns	
	Specification	
Typical SUT signal loading	**AC Impedence**	**DC load**
Signals: DQA: 8–0, DQB: 8–0, COL: 4–0, ROW: 2–0,	28 Ω	(2) 10E451
Signals: CFM, CFMN	28 Ω	(2) 10EP11
Signals: CTM, CTMN	28 Ω	None
Signals: SCL, SWP, SDA, SA0, SA1, SA2,	None	None
Signals: SIO, SCK, CMD	28 Ω	(1) XCV300

1 **The SCK clock rate cannot be more than one quarter the Rambus clock rate.**

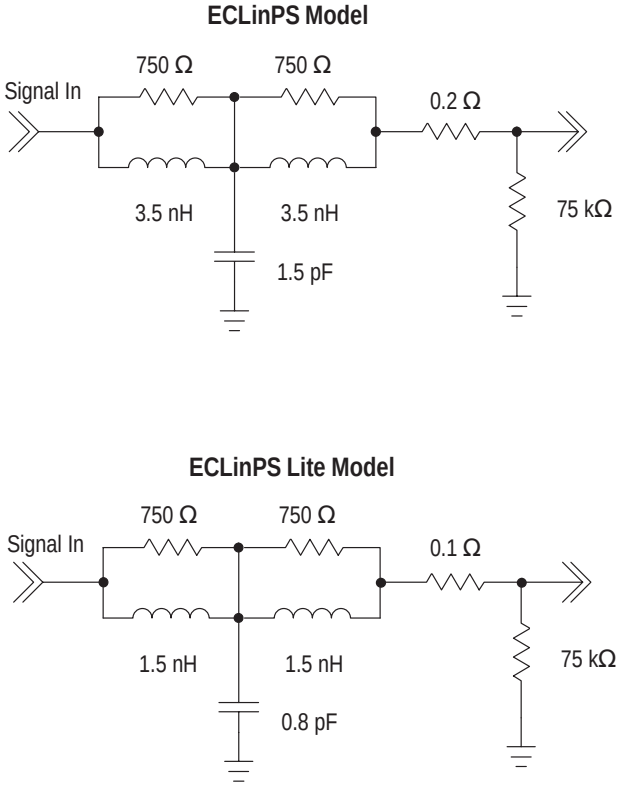


Figure 3–1: Electrical load model

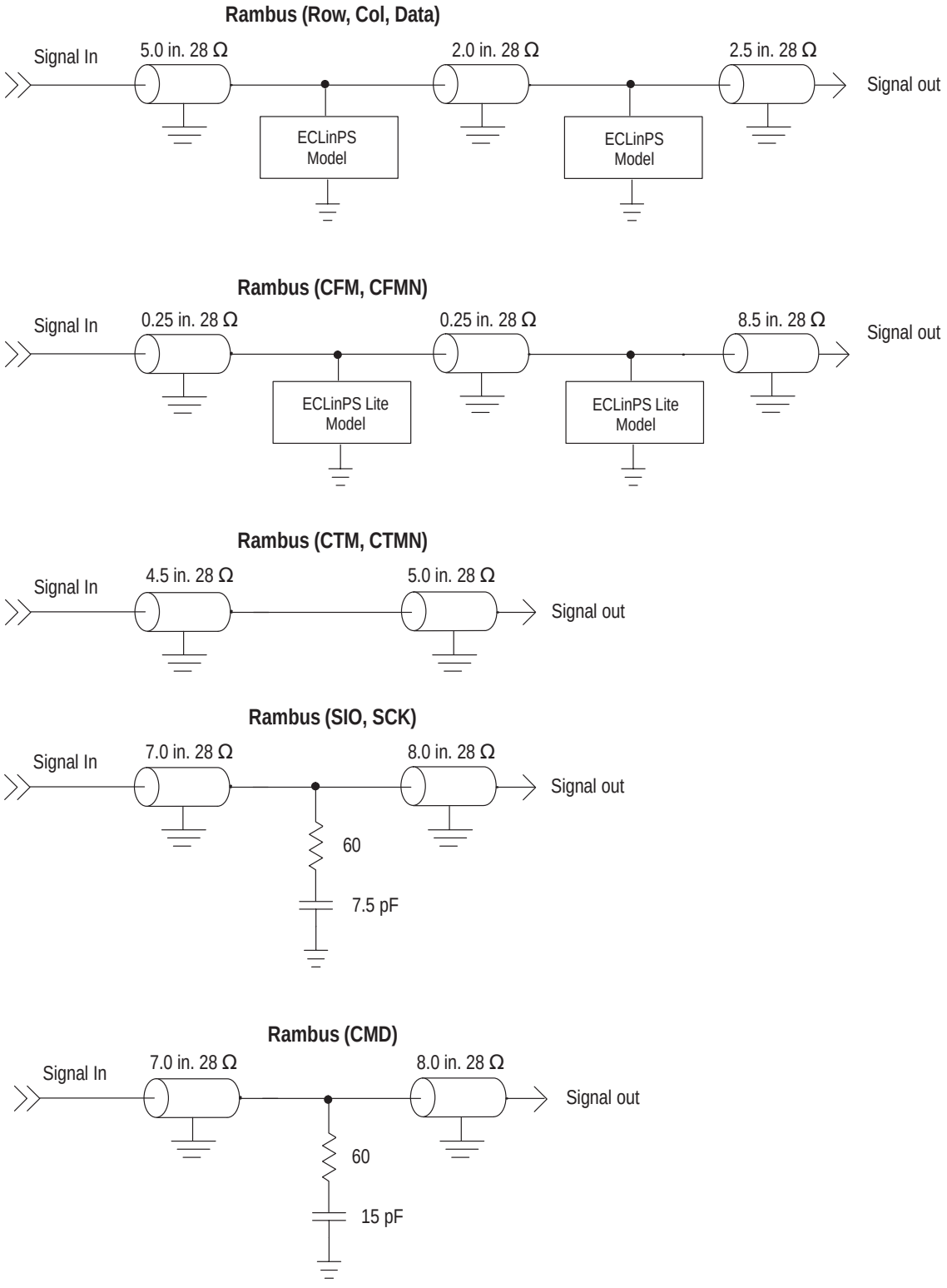


Figure 3–2: Electrical load model

Dimensions

Figure 3–3 shows the dimensions of the Rambus Direct probe adapter.

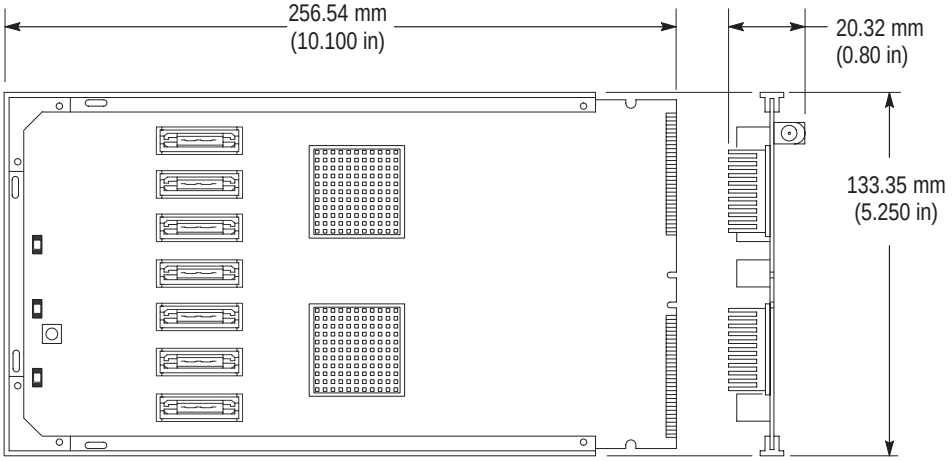


Figure 3–3: Dimensions of the Rambus Direct probe adapter

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all safety summaries before performing any service.

Maintenance

Maintenance

This section contains information on replacing the Rambus Direct probe adapter fuses.

Replacing the Fuse

If a fuse on the probe adapter opens (burns out), you can replace it with a 7 A, 125 V fuse. Figure 4–1 shows the location of the fuse on the Rambus Direct probe adapter. See the *Replaceable Parts List* chapter for part descriptions.

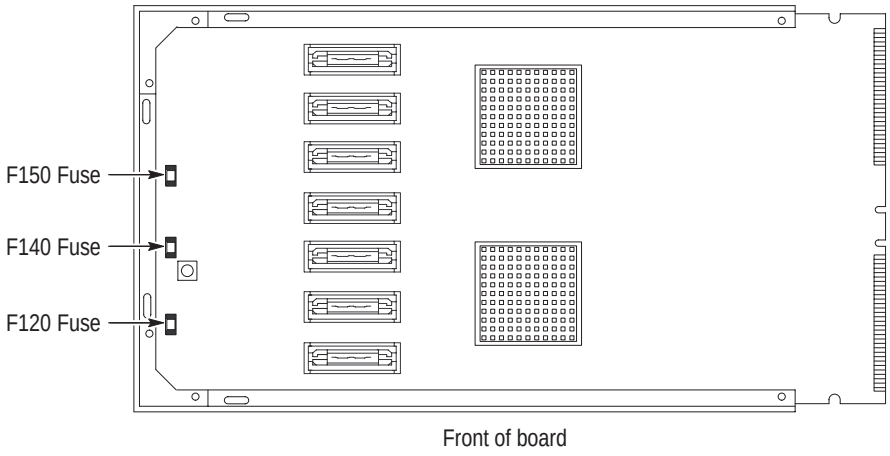


Figure 4–1: Fuse location on the Rambus Direct probe adapter

Diagrams

Replaceable Parts List

Replaceable Parts

This section contains a list of the replaceable parts for the TMS 810 Rambus Direct support product.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105–3608
13103	THERMALLOY INC	2021 W. VALLEY VIEW LN PO BOX 810839	DALLAS, TX 75381–5381
60381	PRECISION INTERCONNECT CORP.	16640 SW 72ND AVE	PORTLAND, OR 97224
75915	LITTELFUSE INC	800 E NORTHWEST HWY	DES PLAINES, IL 60016–3049
82389	SWITCHCRAFT	DIV OF RAYTHEON 5555 N. ELSTON AVENUE	CHICAGO, IL 60630–1314
31918	ITT SWITCH PRODUCTS	8081 WALLACE RD	EDEN PRAIRIE, MN 55344–8798
14310	AULT INC	7300 BOONE AVE NORTH BROOKLINE PARK	MINNEAPOLIS, MN 55428

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
5–1–1	671–5042–00			1	CIRCUIT BD ASSY:RAMBUS DIRECT RIMM MEMORY BUS PROBE ADAPTER, TMS810 01	80009	671–5042–00
–2	131–6610–00			3	JACK,POWER DC:PCB,MALE,RTANG,2MM D PIN,BRASS,SILVER PLATE,5A,	82389	RAPC722TB
–3	214–4571–00			2	HEAT SINK,SEMIC:IC,PGA 13X13/TEQ100,1.235 X 1.3 X 0.65 H,PIN FIN,ALUMINUM,BLACK ANODIZED,2326B	13103	2326B
–4	131–6134–01			7	CONN,RCPT:SMD,MICTOR,FEMALE,STR,38 POS,0.025 CTR,0.240 H,W/0.108 PCB HOLD DOWNS.PALLADIUM	00779	767054–1
–5	105–1089–00			7	LATCH ASSY:LATCH HOUSING ASSY,VERTICAL MOUNT,0.48 H X 1.24 L,W/PCB SINGLE CLIP,P6434	60381	105–1089–00
–6	159–5010–00			3	FUSE,SMD:7A,125V,FAST BLOW,0.1 X 0.1X 0.24,UL REG,CSA CERT,	75915	451007
–7	260–2280–00			1	SWITCH,SIG:SPST,MOM,NO,W/OUT GND TERM, MANUAL INSERT,300 GRAMS,SILVER,SEALED	31918	KSA0M411
					STANDARD ACCESSORIES		
	071–0471–02			1	MANUEL,TECH: INSTRUCTION;TMS810,DP	80009	071–0471–02
	119–5061–01			3	POWER SUPPLY:25W,5V 5A,CONCENTRIC 2MM,90–265V,47–63 HZ IEC,15X8.6X5 CM, UL,CSA, TUV,IEC,SELF	14310	SW108KA0002F01
	161–0104–00			3	CA ASSY,PWR:3,18 AWG,98 L,250V/10AMP,98 INCH,RTANG,IEC320,RCPT X STR,NEMA 15–5P,W/CORD GRIP	S3109	ORDER BY DESCRIPTION
					OPTIONAL ACCESSORIES		
	————————*			7	P6434 MASS TERMINATION PROBE, Opt 21 *	80009	P6434
	161–0104–05			3	CA ASSY,PWR:3,1.0MM SQ,250V/10A,2.5 METER,RTANG,IEC320,RCPT,AUSTRALIA,SAFTEY CONTROLLED,	TK1373	ORDER BY DESCRIPTION
	161–0104–06			3	CA ASSY,PWR:3,1.0MM SQ,250V/10A,2.5 METER,RTANG,IEC320,RCPT,EUROPEAN,SAFTEY CONTROLLED	TK1373	ORDER BY DESCRIPTION
	161–0104–07			3	CA ASSY,PWR:3,1.0MM SQ,240V/10A,2.5 METER,RTANG,IEC320,RCPT X 13A,FUSED,UK PLUG,(13A FUSE)	TK2541	ORDER BY DESCRIPTION
	161–0167–00			3	CA ASSY,PWR:3,0.75MM SQ,250V/10A,2.5 METER,RTANG,IEC320,RCPT,SWISS,NO CORD GRIP,SAFTEY CONTR	S3109	ORDER BY DESCRIPTION

*** Check the P6434 manual for detailed replaceable part number information.**

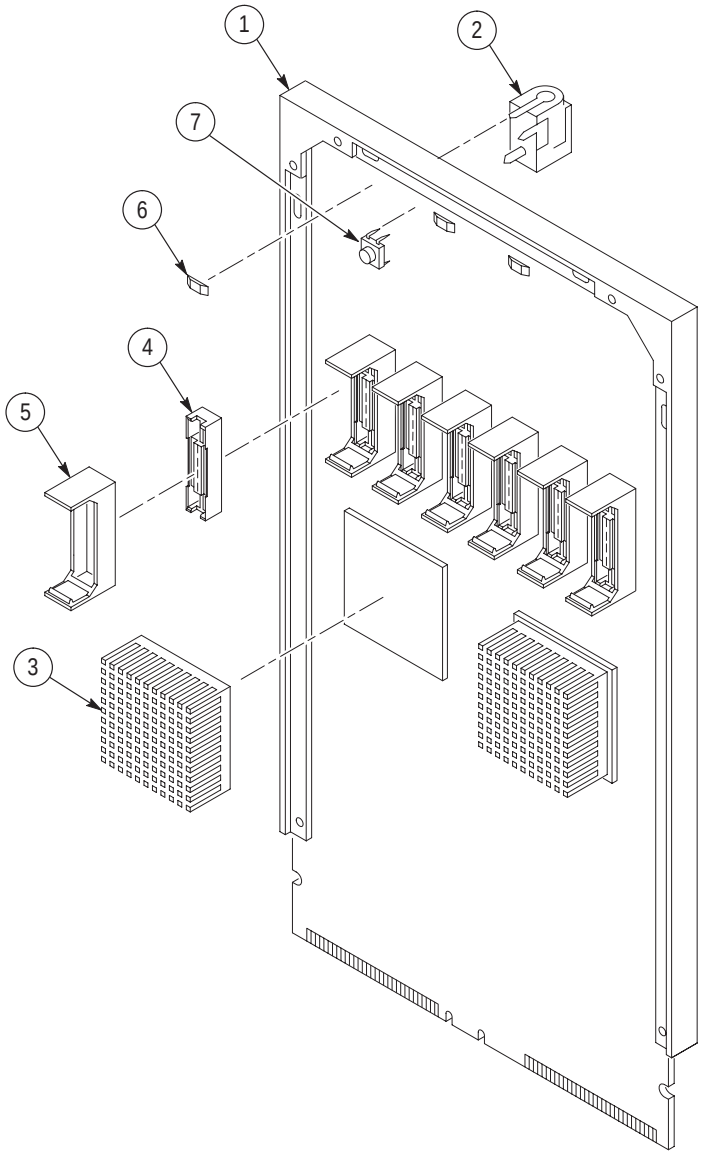


Figure 6–1: TMS 810 Rambus Direct probe adapter exploded view

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